Ph.D. DISSERTATION

Silicon Nanowire Tunneling Field-Effect Transistor Compatible to Complementary Metal-Oxide-Semiconductor Technology

CMOS 소자와 함께 쓸 수 있는 실리콘 나노선 터널링 전계효과 트랜지스터

BY

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지도교수 박 병 국

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ABSTRACT

In order to develop practical low-power switching devices operating at a voltage below 0.5 V and solve the power density problem of highly-scaled CMOS technology, the silicon nanowire band-to-band tunneling field-effect transistors (TFETs) and conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) are co-integrated with a modified CMOS flow and their electrical functionalities are confirmed.

Since the carrier injection in a TFET system occurs by tunneling of valence-band electrons, it can operate without leakage issue and the gate bias swing to switch the device can be very small. In spite of the fancy operating principles, however, the replacement of MOSFETs with TFETs is not likely to happen in near future. This is because the difference of source/drain (S/D) polarities and current-flow directionality issues make TFETs not suitable for the existing MOSFET-based CMOS circuits but demanding new circuit topologies. Therefore the TFETs that can be co-integrated with MOSFETs are selected as the topic of this work.

From the theoretical study with a TCAD device simulator, the gate insulator thickness, nanowire width, abruptness of doping profile near the source/channel boundary and the design of sidewall spacer width are found to be critical to reducing the tunneling barrier width to increase the current. Design concepts learned from TCAD simulation

studies are implemented to fabrication with a novel integration scheme for self-aligned asymmetric S/D. By inserting the process steps to form the asymmetric S/D to the conventional CMOS process flow, MOSFETs and TFETs are successfully co-integrated on the same silicon-on-insulator substrate. Through newly developed and optimized processes such as reduced-repulsion electron-beam lithography, chemical corner-rounding, tight sidewall spacer etch, and two-step self-aligned nickel silicide process, the TFETs with L = 1 μm ~ 28 nm, minimum W = 14.5 nm, 20 nm dual sidewall spacer, and dopant-segregated steep doping profile are successfully fabricated.

From the electrical measurement of gate-induced drain leakage (GIDL) of the co-integrated MOSFETs, the impurity profile near the n^+/intrinsic boundary is found to be much more abrupt than near p^+/intrinsic boundary. Therefore, the fabricated TFETs operate better as a p-channel device rather than n-channel device. The long-channel device shows good switching characteristics of 47 mV/decade. Short-channel effect similar to that of MOSFETs is experimentally observed for TFETs. It is also demonstrated that the short-channel effect can be reduced by improving electrostatics, with a thinner-nanowire device with L = 109 nm. Substrate-bias controllability of TFETs and its extension to nanowire TFETs are examined in the comparison with MOSFET's. Possibilities to improve current drivability by controlling tunneling process with the channel direction are explored with both planar and nanowire TFETs.

From this study, it is demonstrated that TFETs can be co-integrated with CMOS devices in a more manufacturable way by introducing a self-aligned integration scheme to

conventional process flow. This work also opens a possibility of a new low-power design technology using MOSFET/TFET hybrid circuits.

Keywords: band-to-band tunneling field-effect transistor, nanowire transistor, self-aligned asymmetric source/drain, co-integration, CMOS compatibility, sub-0.5 V operation.

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CONTENTS

Chapter 1

Introduction

1.1 Origin of Power Crisis in CMOS Technologies

From desktop computers to smart phones or even to wearable computers in near future, the demands for more functions in smaller devices with higher portability are pushing the chip density to the extreme. As a result, the power density problem has become more and more important. Then this power problem is directly related to the scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs). Since the carriers are injected to the channel through statistical process in a MOSFET system, the leakage current is an exponential function of threshold voltage (V_T) or $\exp(-V_T/mk_BT)$. Therefore, the scaling of V_T leads to a dramatic increase of the stand-by current of MOSFETs. Meanwhile, the operation voltage (V_{OP}) cannot be reduced without V_T scaling, because V_{OP} - V_T determines the current drivability of the device (Fig. 1.1).

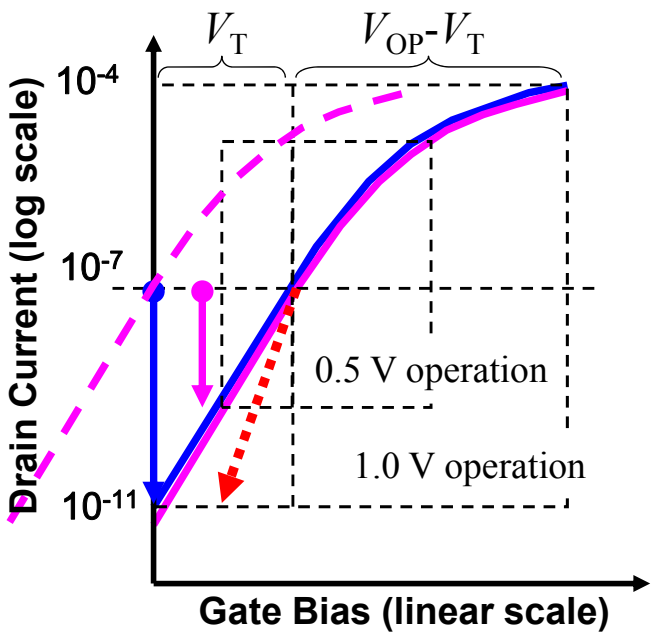


Fig. 1.1. V_T and V_{OP} scaling problem.

Difficulty of V_{OP} scaling leads to that of the operating power reduction.

Another reason why V_{OP} scaling for MOSFETs is not easy is related to the operation principles. A MOSFET gates a current by controlling the polarity of the semiconductor region between the source and drain (S/D). In other words, it means that the gate voltage swing should be larger than 0.56 V or half of bandgap energy at least to switch MOSFETs.

Presently, there are two approaches to overcome the on/off-current trade-off and V_{OP} scaling issues. One is to use the low-power design technologies from circuit design perspective; multiple threshold CMOS (MTCMOS), substrate-bias controlled variable

threshold CMOS, and clock-gating for example [1-3]. These techniques optimize the uses of devices without fixing the device itself. The other is an approach from the device perspective. New materials and structural changes are adopted to improve the device and reduce V_{OP}. Strained technology and slow-down of physical oxide scaling (90nm), high-κ/metal gate (45 nm), and tri-gate devices (22 nm) are such examples [4]. In spite of all these efforts, still V_{OP} of the latest technology remains at 0.75 V and V_{OP}-scaling below 0.6 V is very challenging at this moment [5].

In summary, in order to solve V_{OP} scaling and power crisis problems fundamentally, a new device showing a large subthreshold current change with a small change of gate voltage is necessary.

1.2 Tunneling Field-Effect Transistors (TFETs)

Tunneling field-effect transistor (TFET) is one kind of field-effect transistor using band-to-band tunneling mechanism to inject carriers into the channel region. At off-state, the energy of valence electrons in the source region is bounded and there are no available states on the other side of tunneling barrier. Therefore leakage current is minimized. As the energy band goes down with the gate bias, the valence electrons start to 'see' the empty states across the barrier. If the energy barrier becomes thin enough, the valence electron in the source region start to appear on the other side of the tunneling barrier and large current start to flow. Since the device does not require large switching voltage to

Table 1.1. Some features of TFETs compared with MOSFETs'.

	MOSFET	TFET	Results
Carrier injection mechanism	thermal injection over gate-controlled energy barrier	tunneling through gate-controlled energy barrier	abrupt transition between off and on states but smaller current drivability
S/D polarity	same	opposite	difficulty in self-aligned integration and area penalty for stacked circuit topology
Current flow direction	bi-directional between S & D	one-directional	not useful for data access device

maintain small off-current, it is suitable for low voltage operation.

Since the first experimental demonstration of sub-60 mV/decade with a Si-based TFET in 2007, many researchers have been evaluating TFETs of various structures and reporting important challenges of the devices [6-8] (Table 1.1). First, the current drivability of TFETs is too small due to large tunneling resistance, and usually the current cannot reach even 1 μA/μm. Considering typical MOSFETs can drive a current more than 700 μA/μm, this is very small value. Second, the polarity of source and drain regions are the opposite. Interestingly enough, TFETs can operate as both n- and p- channel devices thanks to this unique feature. However, the difference of S/D polarities makes it impossible for TFET to work as the data access node device and self-alignment is difficult. As a result, the fabrication procedures of TFETs tend to be incompatible to

CMOS process flow or gate length scaling is subjected to the overlay error limitation of the photolithography equipment. These issues of the current drivability, needs of new circuit topology, and compatibility of integration flow are the important reasons why TFETs still remain as exploratory device. However, there is another important aspect to consider using TFETs in CMOS technology.

1.3 Replacer or Complementor?

As the technology node goes beyond 90 nm and development cost of new technology rapidly increases, the CMOS technology industry is experiencing structural change [9, 10]. That is, many integrated device manufacturers (IDMs) gave up their fab-ownership to focus on chip design. Instead more specialized fab companies (foundries) started to appear to take responsibility for manufacturing of the chips (Fig. 1.2). As a result, the industry ecosystem is being re-organized to be the vertically-structured external business where fabless firms and foundries are playing the key roles. Considering the complexity of modern microelectronics chips and the productivity of the design work, the automation and re-use of designs from the previous technology node are indispensable to designers. Therefore, such structural changes in industry have resulted in stronger resistance against any unique changes which makes the re-use of previous designs difficult. From this viewpoint, TFETs are not likely to replace MOSFETs near future due to their poor current drivability and unique topological restrictions.

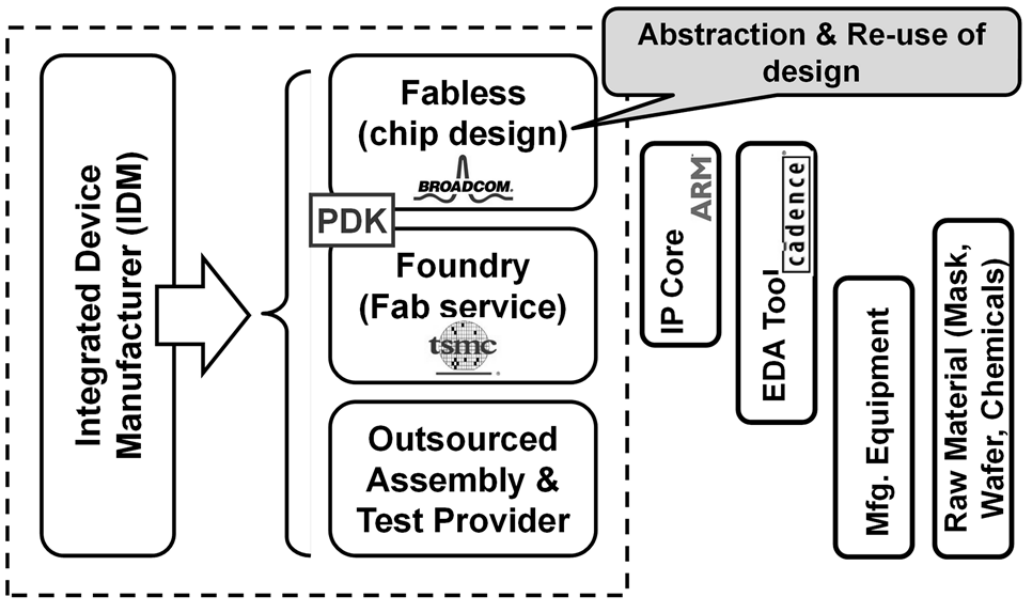


Fig. 1.2. Re-organized ecosystem of microelectronics industry.

Table. 1.2. MOSFET/TFET hybrid low-power design.

	Conventional MTCMOS method	Hybrid MOSFET/TFET method
Devices on timing-critical paths	low V_T device	MOSFET
Devices out of timing-critical paths	high V_T device	*TFET

* only for one-directional switching devices.

After all, a more probable way that TFETs are accepted to CMOS technology will be to use them as complementors for MOSFETs. In other words, constructing energy-efficient MOSFET/TFET hybrid circuits to assign TFETs at infrequently-switching uni-directional components will be one of the possible options to use TFETs in CMOS technology [11] (Table 1.2).

1.4 Previous Studies

Previous researches on TFETs from the earliest year to 2009 are well summarized in two papers [7, 8]. The focus of the early works was mostly on how to demonstrate the excellent switching properties of sub-60 mV/decade. However, since there were no process options to induce strong electric field within the semiconductor region in Si CMOS technology before 2008, the fabricated devices seldom achieved such low subthreshold swing values [6, 12]. Therefore, TCAD simulation played an important roles in evaluating the devices of experimental designs and materials during this time [13]. It was revealed that the sequential turning-on of junctions due to the graded doping concentration of the source region and electric field shielding is responsible for the apparent poor swing of early TFETs also [14].

It is since the effective EOT decreases to or below 3 nm with the help of high-κ gate dielectrics and the geometric effect of the nanowire channel that many results of sub-60 mV/decade started to be reported [15-18]. Not only Si but also other narrow bandgap

materials were evaluated for the further improvement of swing and the drive current boosting. These materials are SiGe, Ge, GeSn, carbon nanotube, graphene, and indium-containing III-V materials. [19-26]. Among these materials, however, the material compatible to the present CMOS technology is only SiGe as of 2013. In addition, a self-aligned integration scheme to form these materials only on the source or channel regions to prevent the unwanted leakage around the drain edge is not developed [19]. Therefore, a practical performance improvement using narrow-bandgap materials will still need a lot of work.

With the consideration of a TFET as the beyond-CMOS device after the MOSFET, its characteristics started to be reviewed from various aspects [27]. Through these works, some unique problems or limitations of TFETs were highlighted aside from the poor current drivability.

One of such examples is the one related to scalability. Due to the asymmetric configuration of the S/D, dopings of the S/D regions need to be done separately, which restricts the gate length scaling due to the overlay variation of S/D photolithography processes. The smallest gate length of fabricated planar TFETs is demonstrated to be around 200 nm [28]. Using the vertical-channel configuration was proposed as other way to solve the scalability problem [11, 13, 16, 17, 29, 30]. Clearly, this approach has many benefits in that it can reduce the dimension of the devices without concerns on the overlay issues and the choice of the source material is free. The greatest challenge with the approach may be on the difficulty of interconnection though: In the real fabrication, there

occurs the level difference between the source and the drain. Since the dimension of plug contacts shrinks with the technology node, connecting electrodes at different levels will be very challenging and may require some unique integration schemes [16, 17]. An increase of series resistance due to scaling of S/D thickness is another concern. From this respect, the designs using mesa-structure is expected to have similar interconnection problems [6, 29, 31].

Issues in constructing circuits with TFETs were also found. The typical examples include large Miller capacitance, occurrence of glitch in the transient characteristics, weaker inverter cell stability [11, 32-34]. Also, a need of special circuit topology due to the asymmetric current flow was reported [32, 35].

1.5 Thesis Outline

On the basis of discussions so far, the nanowire TFETs which can be co-integrated with the MOSFETs and the fabrication method are chosen as the topics of this work. The conventional CMOS technology is modified to co-integrate nanowire MOSFETs and nanowire TFETs. Chapter 2 will cover the theoretical background of TFETs. Through TCAD simulation study on the model nanowire devices, operating principles, operation characteristics unique to TFETs are to be highlighted. In addition, variability on several design parameters is investigated and the critical parameters for the fabrication of devices are clarified. From this study, the structure of target device is defined. In Chapter 3, after

the overall process flow for the fabrication is briefly introduced, the key modules are explained in detail. Here, a method to form sub-20 nm nanowire array with a novel rounding method is to be reviewed. A novel self-aligned integration scheme for asymmetric S/D and optimized self-aligned silicide process are explained. Chapter 4 is dedicated to show the electrical test results of the fabricated devices. In addition to the analysis on the device components, the design split results such as wire-width dependence, short-channel effect, and back-gate effect are examined. As a potential knob for the further device improvements, the effect of channel direction is briefly examined. In the final chapter, Chapter 5, this work will be concluded with summary and interpretation of the results suggesting the direction of the future work.

Chapter 2

Theoretical Studies

In this chapter, the operation principle of TFETs, the effect of active dimension scaling, and device variability are studied with TCAD device simulation. For the improved reliability of the simulation results, the calculation is performed with the non-local band-to-band tunneling model with Sentaurus Device (version G-2012.06) of Synopsys Inc. after confirming that the model with experimental secondary ion mass spectroscopy data and the measured *I-V* characteristics show a good agreement [36, 37]. Since the simulation tool automatically calculate the tunneling current with the consideration of valence band gradient, more accurate result is obtained [38].

2.1 Basic Operations of TFETs

The operation of a TFET can be understood more easily with Zener breakdown of a gated p-i-n diode. If the gate bias induces strong band bending near highly-doped source/channel boundary region, valance electrons from source region start to tunnel the barrier and appear in the channel region. Figure 2.1 conceptually shows the energy bands

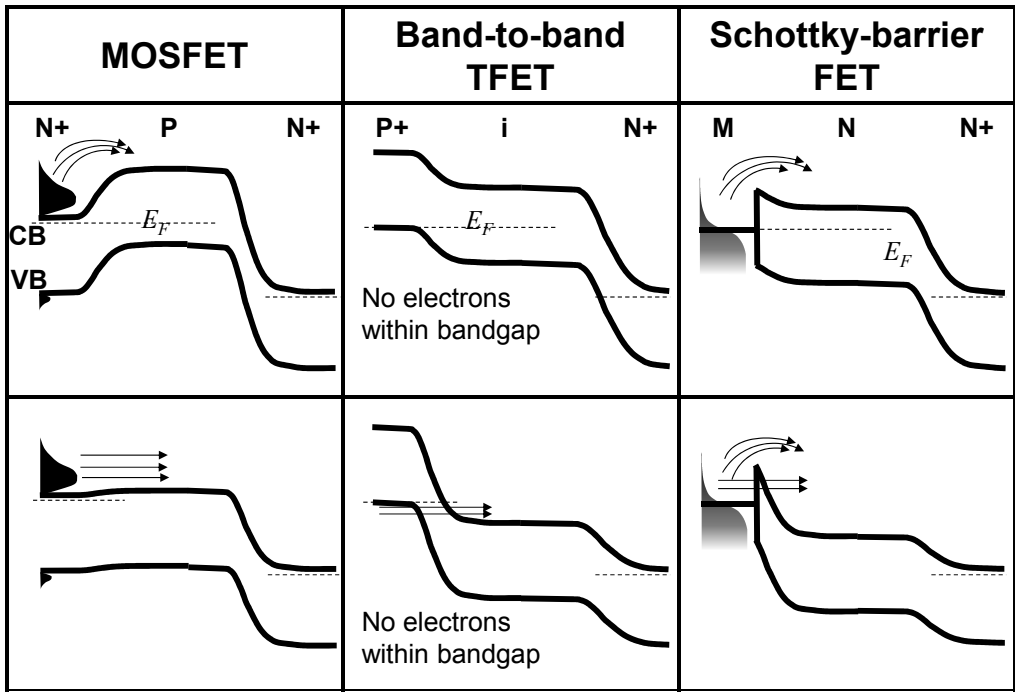


Fig. 2.1. Change of energy bands of three devices during operation.

of a MOSFET, a TFET and a Schottky-barrier FET (SB-FET) during operation. At off-state, there is no upper limit of carrier energy in the source regions of the MOSFET and SB-FET. Current injection of such tail electrons is hard to control and needs a large gate bias change to turn off. Meanwhile the energy of the injected electrons in the TFET system is bounded to valence band maximum. Therefore the chance of current leakage by high energy carrier is completely excluded and very sharp on-off transition is possible with TFETs. Although SB-FET also uses tunneling mechanism for the current flow at on state, it is difficult to prevent the unwanted off-state leakage current due to unbounded carrier energy distribution at off-state. Figure 2.2 is the simulated transfer characteristics

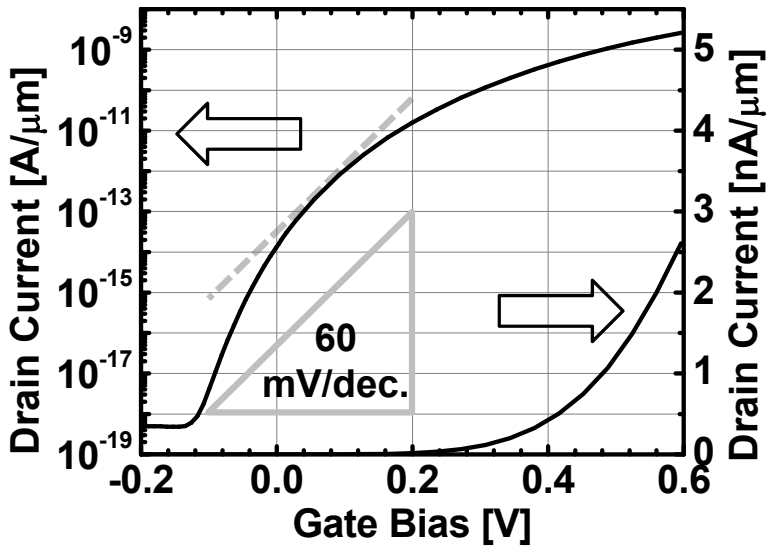
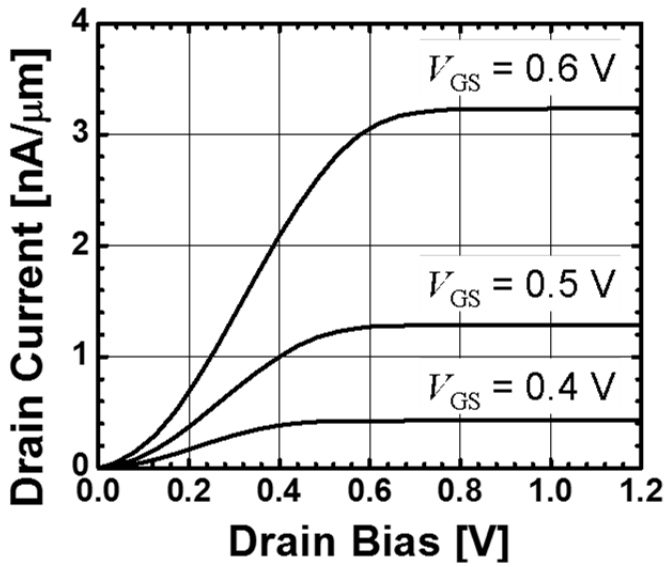


Fig. 2.2. Transfer characteristics of the model TFET. Here V_{DS} = 0.5 V.

of a gate-all-around (GAA) nanowire TFET as an example. Here the dimensions of the active and gate are set to be 10 nm in width and 22 nm in length, respectively. As explained with energy band diagram, a very sharp on-off transition with a point swing of sub-60 mV/decade is observed. This shows the great potential of TFETs as low-power device operating at 0.5 V and below. Unlike the subthreshold slope of a MOSFET, the $d\log_{10}(I_D)/dV_{GS}$ of TFETs continuously increases as the gate bias decreases.

Figure 2.3 is the simulated output characteristics of the model TFET. Since total current is determined not by the channel resistance but the tunneling resistance, large drain bias is needed for the current to saturate and the saturated current values show large sensitivity to the gate bias. Although the apparent current saturation behavior of the TFET looks similar to that of a typical MOSFET, the physics behind the phenomena is quite



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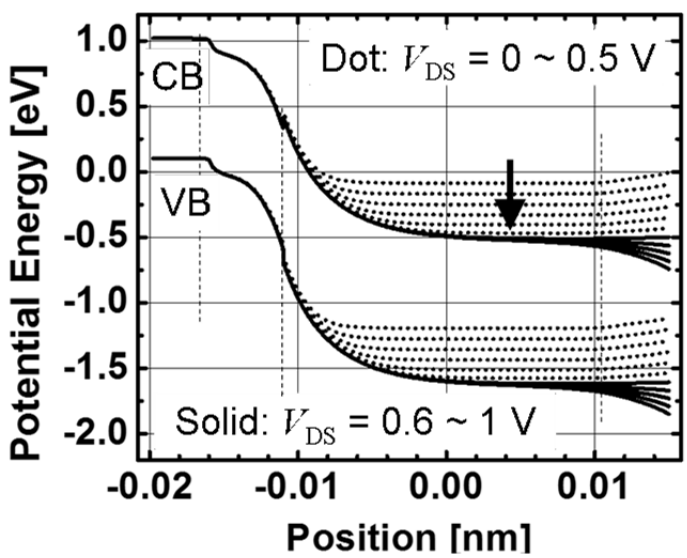


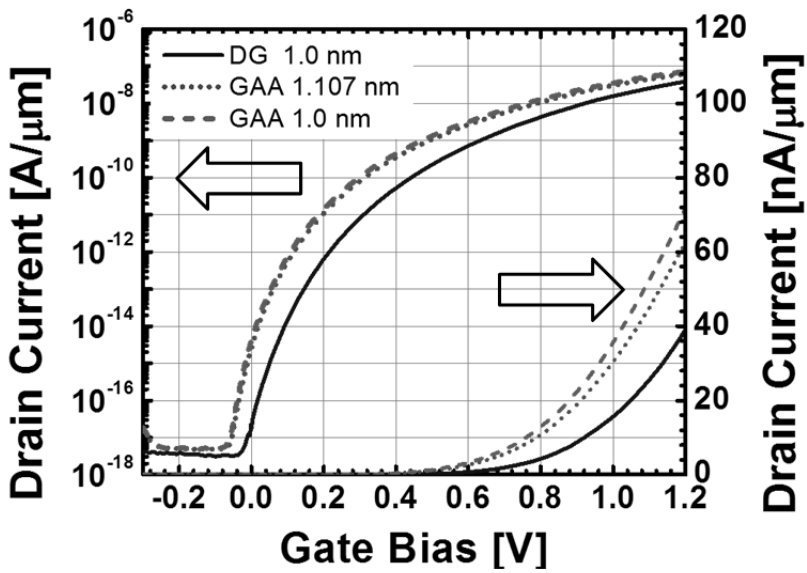
(b)

Fig. 2.3. (a) Output characteristics of the model TFET. (V_{DS} = 0.5 V) and (b) energy band diagram near source region with V_{GS} = 0.5 V

different. While the current saturation of MOSFETs occurs due to the disappearance of inversion layer from the drain-side edge, the inversion layer of TFETs is electrically tied to the drain and disconnected from the source until it reaches the saturation point. The current saturation of TFETs occurs when the source/channel depletion region expands to the most of the channel region. Once this happens, only the un-depleted region near the drain is electrically-controlled by the drain bias. Therefore the field near source-side tunneling barrier remains unchanged. Since the field across the barrier does not change, the tunneling current remains constant.

2.2 Nanowire TFETs

In a nanowire field-effect transistor system, the gate capacitance of the device appears as if the gate insulator thickness were reduced by a factor of $\ln(1 + T_{\mathrm{ox}}/R)^{R/T_{\mathrm{ox}}}$ due to the geometric benefit. In addition to this effect, the field coupling also plays an important role in nanowire actives. Figure 2.4 shows the field-coupling effect by comparing three devices; 10 nm-body double-gated TFET with 1 nm gate oxide layer, 10 nm-wide GAA nanowire TFET with 1.107 nm gate oxide, and 10 nm-wide GAA nanowire TFET with 1 nm gate oxide. The areal gate capacitance of a nanowire field-effect transistor with W = 10 nm and T_{OX} = 1.107 nm is same as the one of planar system with T_{OX} = 1 nm. An interesting result is that not only the nanowire device of the same physical oxide thickness shows superior transfer characteristics over the double gate device but also the nanowire device of the capacitively equivalent gate oxide also



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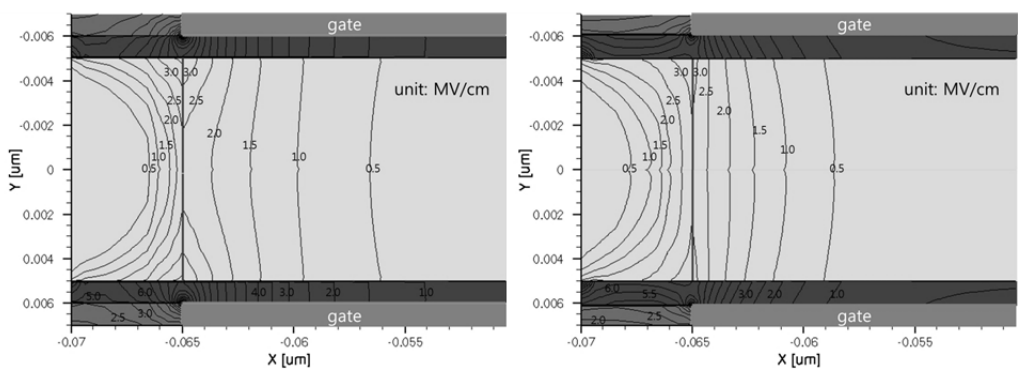


(b) (c)

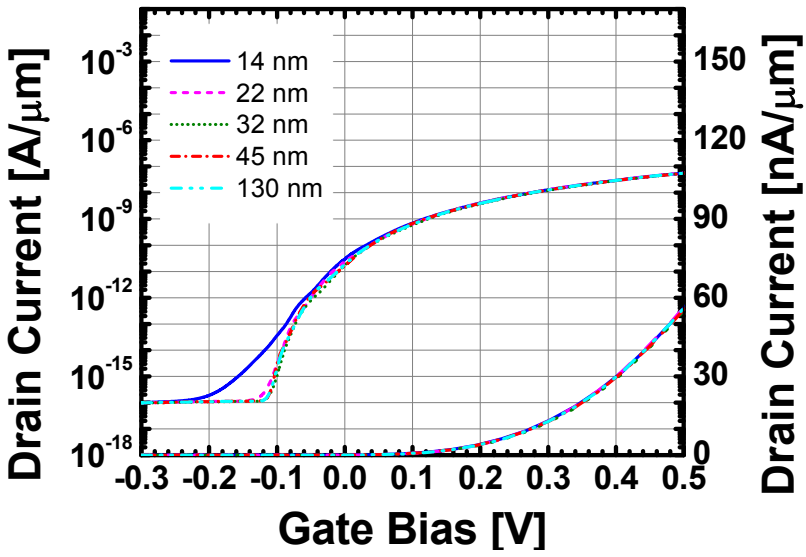
Fig. 2.4. (a) Transfer characteristics of three TFETs: double gate TFET with T_{OX} = 1 nm, GAA TFET with T_{OX} = 1.107 nm, and GAA TFET with T_{OX} = 1 nm (V_{DS} = 0.5 V, L = 0.13 μm), (b) electric field contour of double gate TFET, (c) electric field contour of GAA TFET with T_{OX} = 1.107 nm. Here V_{GS} = V_{DS} = 0.5 V.

outperforms the double gate device. The clue to understand this phenomenon is in the electric field contour diagrams. Although the physical oxide is thicker, the gate electric field of the nanowire system influences deeper region inside the wire and the field is stronger in the center of wire than on the wire surface. This is because the field from the surrounding gate couples in the center of the wire and induces more abrupt band bending. This is a very desirable phenomenon for a TFET system which needs a strong bending near source/channel boundary to improve the tunneling current and switching characteristics.

2.3 Device Design Factors and Variability

From the variability study in this section, how the structural change of a TFET device influences the device characteristics is reviewed. In order to make the results clearer, the behavior of nanowire TFETs is compared with those of the corresponding MOSFETs of the same dimensions. The baseline model device has wire width W = 10 nm and 4 nm-long n^+ doped layer of 3×10^{19} cm^{-3} doping adjacent to the p^+ source region of 2×10^{20} cm^{-3} doping.

First, the transfer characteristics for various gate lengths L are compared in Fig. 2.5. While a slight decrease of L leads to a large increase of I_{OFF} and $d\log_{10}(I_D)/dV_{GS}$ in the case of MOSFETs, the characteristics of TFETs remain unchanged down to 22 nm. These results again show that the channel current I_{DS} of TFETs is dominantly determined by the tunneling resistance. It also implies that TFETs are superior to MOSFETs from the view



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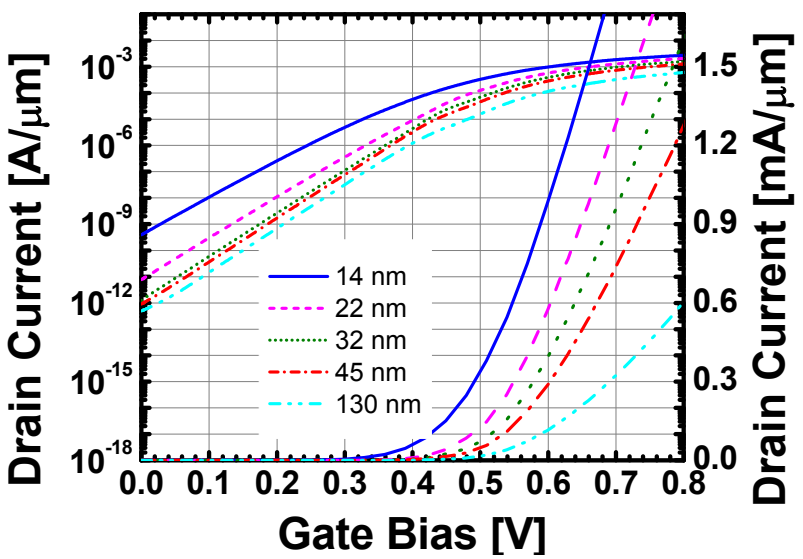


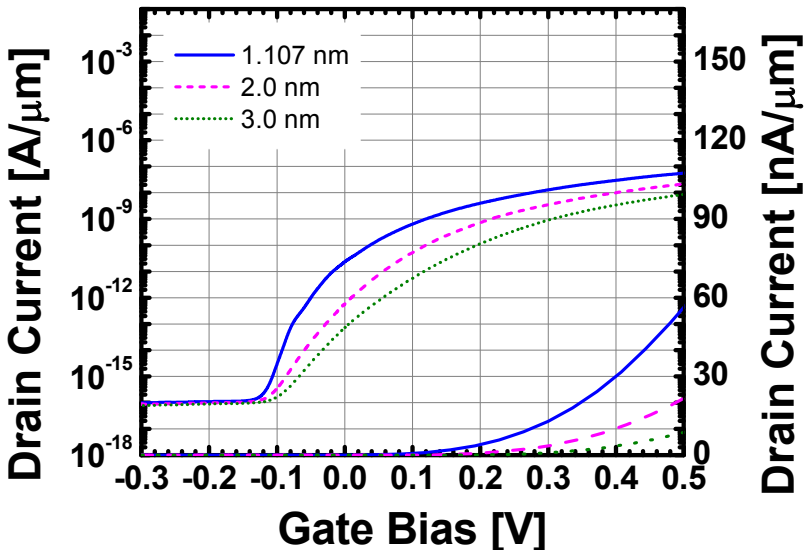
(b)

Fig. 2.5. Transfer characteristics with L variation:
(a) TFET and (b) MOSFET. Here V_{DS} = 0.5 V and T_{OX} =1.107 nm.

point of the gate length scaling, in that the degradation of the off-characteristics is much less sensitive to the channel length scaling and the recessed-channel design considered for highly-scaled technologies will not degrade the current drivability.

Degradation mechanism of I_{OFF} and switching properties of the 14 nm-gate TFET is worthy of examining more carefully. Since TFETs introduce carriers into the channel by tunneling process through the energy barrier, not by the thermal injection over the barrier, the mechanism of the short-channel effect appears in a different way. In case of the MOSFET, the injection barrier height starts to be affected by the field from the drain as the channel length decreases. Meanwhile, it is the barrier width that the field from the drain starts to influence in the short-channel TFET system. This phenomenon is called as drain-induced current enhancement (DICE) or drain-induced tunneling barrier thinning (DIBT) [39-41]. As a result, the simulated degradation of the switching properties reminds us that the short-channel effect should be considered also for TFETs because it is a universal issue of the field-effect transistor system related to electrostatics.

Secondly, the sensitivities to gate oxide thickness are compared in Fig. 2.6. Not only the switching properties under a small gate bias region but also the current drivability in a high gate bias region strongly depends on the gate oxide thickness. This is because the tunneling current of TFETs is a very strong function of the electric field across the tunneling region while the current of MOSFETs is either an exponential function of the gate bias or a weaker function of $V_{GS} - V_T$. Therefore, the *I-V* characteristics of TFETs are very sensitive to variation of the gate oxide thickness.



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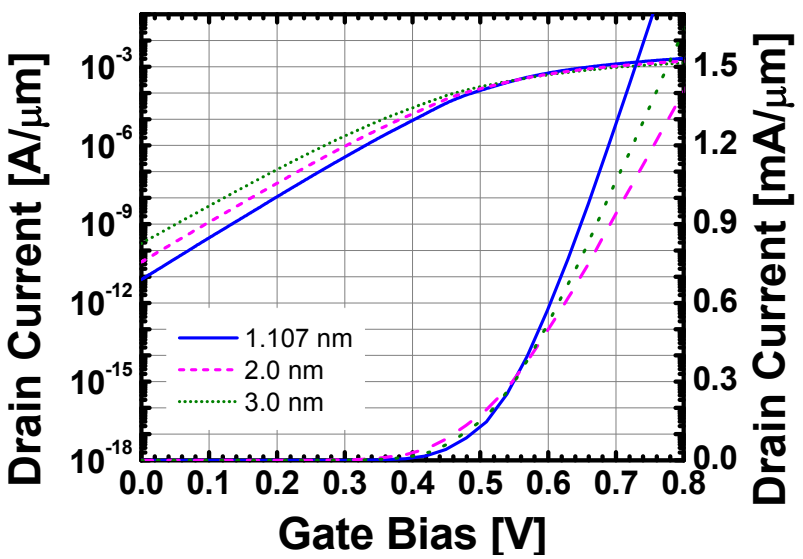


(b)

Fig. 2.6. Transfer characteristics for several different T_{OX}: (a) TFET and (b) MOSFET. Here V_{DS} = 0.5 V and L = 0.13 μm.

Thirdly, the effect of doping profile is studied. Since the tunneling process occurs the depletion region between the source and the channel, making the depletion region as thin as possible will be a way to improve the switching characteristics. Therefore, one may think that this is possible either by controlling the source doping or by controlling the channel-side doping. Actually this is yes and no. In order to understand how the doping profile influences the tunneling process, both the change of the depletion width and the available states for the tunneling process have to be considered (Fig. 2.7). Figure 2.7 (b) shows the case to increase the doping concentration of the source region. Although the increase of the source-side doping level slightly reduces the source-side depletion length, it also increases the number of vacant states in the source region. Therefore, the change of the source doping does not significantly change the switching characteristics. On the contrary, the increase of the channel-side n-type doping does not only decrease the depletion length but also increases the number of vacant states on the channel side. Therefore, the change of I_D-V_{GS} characteristics is much more dramatic (Fig. 2.7 (c)). Figure 2.8 clearly shows this contrast. While an increase of source doping more than 2×10^{20} cm^{-3} have a minor effect on the characteristics, an increase of the doping in the adjacent n-type region significantly improves the switching properties. The length of the adjacent n-type region is varied in Fig 2.9 to understand more on the effect of the degeneracy of the channel region. From the fact that the adjacent region longer than 8 nm cause no further change, the interacting length is thought to be around 10 nm.

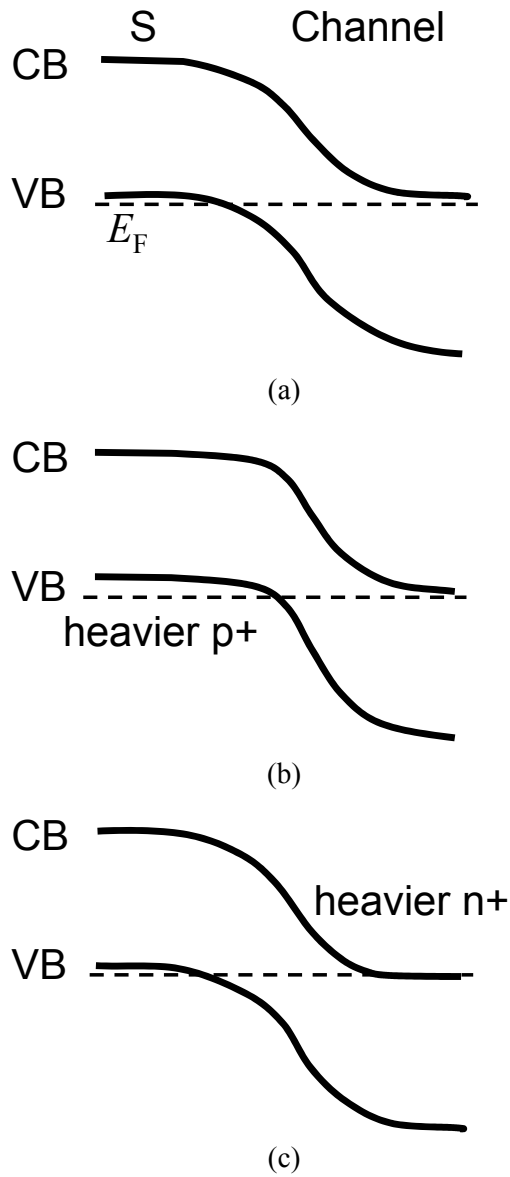
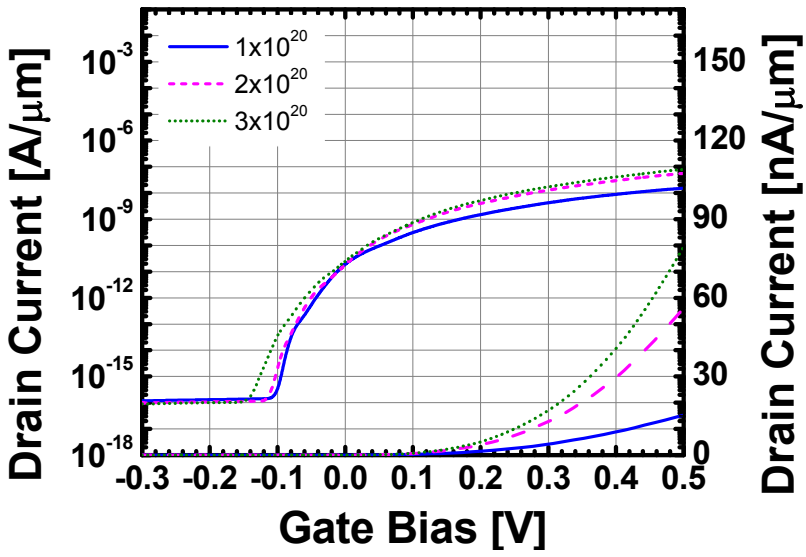
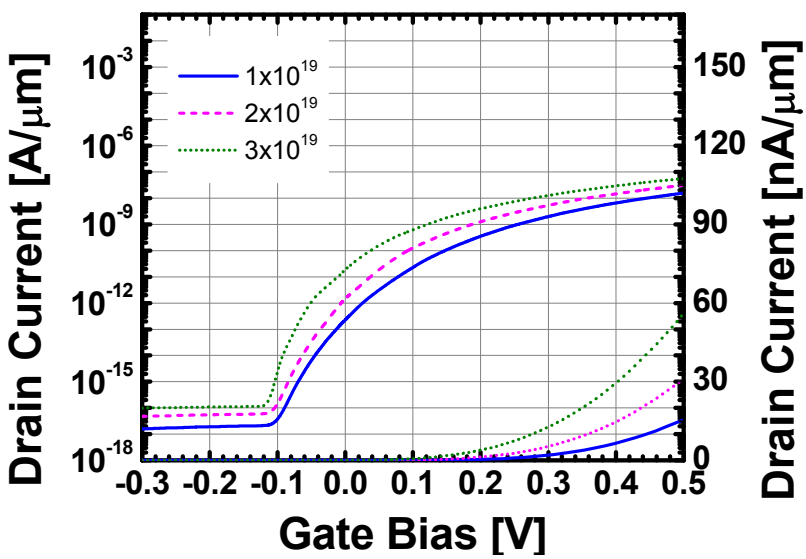


Fig. 2.7. Energy band diagrams for various doping profiles: (a) $N_A = 1\times10^{20}$ cm^{-3}/ $N_D = 1\times10^{19}$ cm^{-3}(control), (b) $N_A = 3\times10^{20}$ cm^{-3}/ $N_D = 1\times10^{19}$ cm^{-3}, and (c) $N_A = 1\times10^{20}$ cm^{-3}/ $N_D = 3\times10^{19}$ cm^{-3}.



(a)



(b)

Fig. 2.8. Transfer characteristics with doping variation: (a) source doping, and (b) adjacent n-type region doping. Here V_{DS} = 0.5 V and L = 0.13 μm.

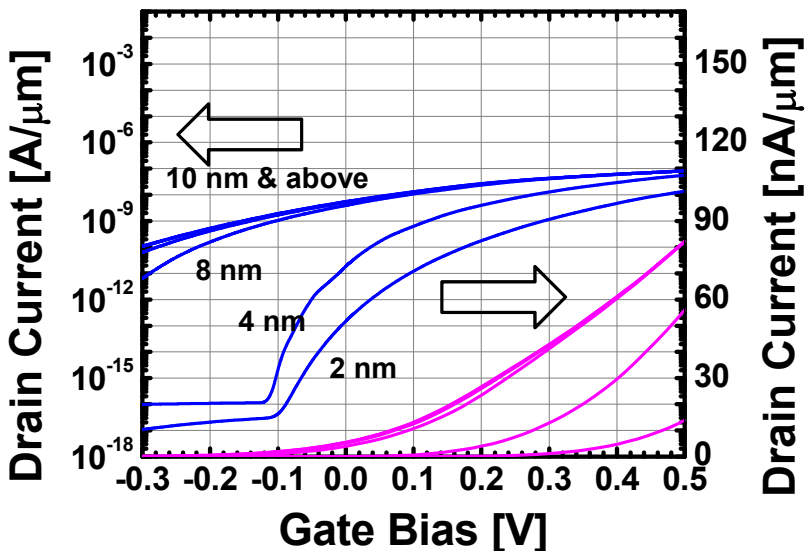


Fig. 2.9. Transfer characteristics with the length of the adjacent n-type region: L_n = 2, 4, 8, 10, 16, and 32 nm. Here V_{DS} = 0.5 V and L = 0.13 μm.

Finally, the effect of the sidewall spacer length can be similarly understood with the change of the tunneling length. A tunneling barrier is formed between the spacer edge and the channel-side depletion edge. As the spacer becomes thinner, the length of the tunneling barrier becomes smaller. Therefore, minimizing the source-side sidewall spacer length improves the driving current of a TFET (Fig. 2.10). On the other hand, adjusting the drain-side spacer length has no effect on the *I-V* characteristics. This implies that the sensitivity to source-side spacer length is not explained by the series resistance but related to the tunneling resistance. Another important point from this result is that the steeper change of doping profile will improve the switching characteristics due to reduced depletion region.

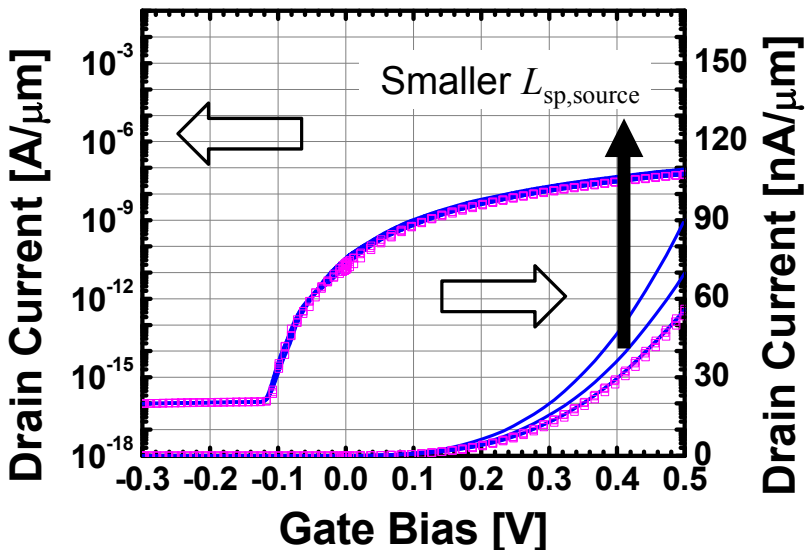


Fig. 2.10. Transfer characteristics with the sidewall spacer length variation: lines: source-side sidewall spacer split with $L_{sp,source}$ = 8, 5, 2, 1 nm symbols: drain-side sidewall spacer split with $L_{sp,drain}$ = 8, 5, 2 nm Here V_{DS} = 0.5 V and L = 0.13 μm.

2.4 Operation Range Where TFETs Beat MOSFETs

As learned from TCAD simulation study on TFETs, the TFET maintains superior $d\log_{10}(I_D)/dV_{GS}$ for a certain range of voltage. This is an important feature from the electrical engineering viewpoint. One cannot design circuits using the devices where the current changes exponentially with respect to the input. Once the gate bias exceeds a certain value, the output current should respond to the gate voltage much more slowly. In order to understand this more clearly, the model GAA TFET and MOSFET are compared as shown in Fig. 2.11.

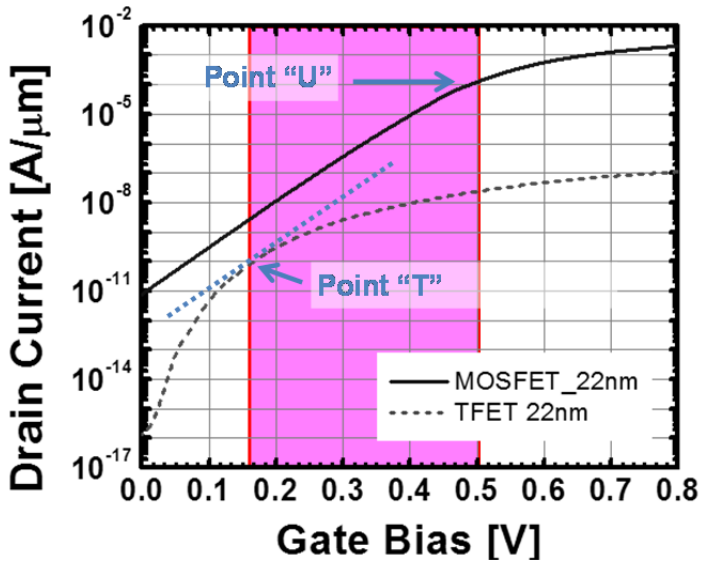


Fig. 2.11. Transfer characteristics of the model MOSFET and TFET: The heights of the two rectangles are equal. Here V_{DS} = 0.5 V.

Here we can see two important points for the comparison. First, there is the point "U" where the exponential behavior of the MOSFET current disappears. It can be considered as V_T of the MOSFET. In Fig. 2.11, the V_{GS} at the point is about 0.5 V. The second point is the point "T", where the tangential swing on the TFET curve becomes 60 mV/decade. Above this point, the current of the TFET changes much slower than that of the MOSFET.

With these points, we can say the model TFET is a more preferred option for low-power circuit design than the model MOSFET, specifically in the range of V_{OP} between 0.16 V to 0.5 V. If V_{OP} is smaller than 0.16 V, the output current of the TFET changes too

sensitive to the input and the merit over MOSFET disappears. If V_{OP} is larger than 0.5 V, the MOSFET can also have slowly varying output current like the TFET in the range. An interesting point is that the point "T" therefore works as V_T of the TFET.

2.5 Summary of Target Devices

From the theoretical consideration so far, the target device of fabrication was defined to have the following features. First, the thickness of the gate insulator and the shape of active region were carefully designed to maximize the electric field from the gate capacitor. The equivalent oxide thickness (EOT) of the gate insulator was selected to be the minimum as long as the gate leakage problem was not serious. Also the channels were formed as nanowire with $W < 30$ nm and the top corners of the channel were rounded to maximize the field-coupling effect and reduce the side-effect of field concentration at the wire corners. Therefore the substrate-bias tunability of the device was also expected to be improved. For the abrupt doping profile near the source/channel boundary region, the length of the sidewall spacer was to be the minimum and the snowploughing effect of silicide was utilized. On the other hand, the drain-side sidewall spacer was designed to long enough to suppress ambipolar effect. Since the possible minimum size of the sidewall spacer and the abruptness of final dopant profile were dependent on the tool performances, the process conditions and the dimensions were optimized during fabrication. The fabrication flow was aimed at demonstrating the co-integration of the TFETs and conventional MOSFETs. Finally, by preparing some TFET devices with the

channel rotated by 45 degree from the normal <100> direction, any possibility of device improvement due to anisotropy of tunneling rates was explored.

Chapter 3

Device Fabrication

3.1 Key Process Designs and Fabrication Flow

In order to co-integrate the proposed nanowire TFETs and MOSFETs without process complexity, the fabrication sequence followed the process flow given below (Fig. 3.1). (a) First, nanowire active patterns were formed on SOI substrates using a well-optimized mix-and-match process of negative-resist electron-beam lithography (EBL) and i-line photolithography followed by reactive ion etch (RIE) and novel corner rounding process. (b) By dry oxidation process at a load-locked furnace and low-pressure chemical vapor deposition (LPCVD) process, the gate film stack of ultrathin silicon oxide (T_{OX} = 2.3 nm) and phosphorus-doped poly-silicon was formed over the active-patterned substrate. (c) The hard mask patterns with a film stack of LPCVD oxide, LPCVD poly-silicon and silicon nitride were formed over the gate film stack to define the asymmetric

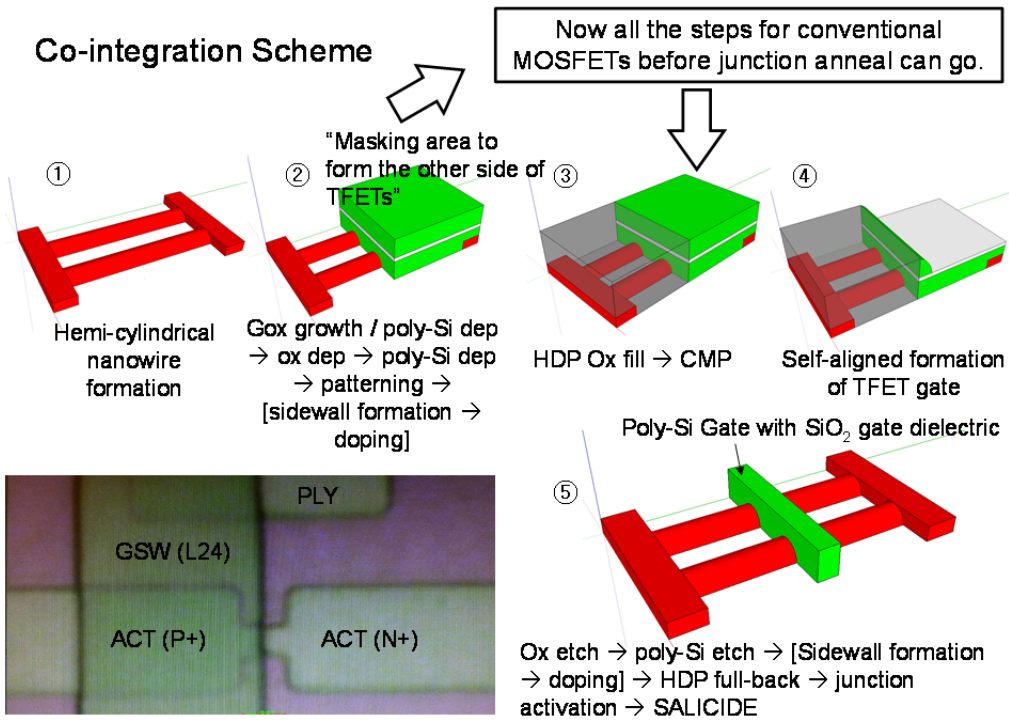


Fig. 3.1. Device fabrication flow.

regions of TFETs. After another mix-and-match process of the hard mask patterns and photolithography, the gates of MOSFET and the first side of the gates of TFETs were formed using carefully-controlled gate RIE process. (d) After forming the first sidewall spacer around the gate patterns, the first implantation processes for MOSFETs and the exposed active regions of TFETs were performed. (e) The hard mask covering the regions of TFETs were opened after deposition of high-density-plasma (HDP) silicon oxide, planarization, and dry etch-back process. After forming etch-masking patterns for TFET gates on the uncovered regions, the second side of TFET gates was formed using

carefully-controlled gate RIE process. (f) Then, the second sidewall spacer was formed with silicon oxide and nitride next to the newly formed sidewall of gates. The second dopants were introduced to the uncovered regions. (g) After HDP oxide was deposited and planarized again, the masking patterns on the gates of TFETs were removed. (h) Finally, after the HDP oxide covering all the other regions was pulled back, the rapid thermal activation of dopants and self-aligned silicide (SALICIDE) processes were performed. By having silicided pads directly connected to devices through silicide, the direct electrical test of the devices were possible right after SALICIDE without any additional processes for interconnection. Device integration was done mostly at the fabrication facility of the Inter-university Semiconductor Research Center (ISRC) located at Seoul National University and some critical processes such as high-selectivity poly-silicon RIE and the growth of ultrathin oxide, phosphorus-doped poly-silicon and other special CVD films, were done with the support of the National Nano-Fab Center (NNFC) in Republic of Korea.

Among the briefly-reviewed integration steps, key highlight modules are explained in more detail in the following sections.

3.2 Patterning and Rounding of Nanowire Active Regions

Thermal oxide of 100 nm was grown on the initial p-type (100) SOI wafers prepared by separation-by-implantation-of-oxygen (SIMOX) process (T_{SOI} = 100 nm and T_{BOX} = 375 nm) and removed to reduce the SOI layer to be 55 nm. Reducing SOI more than this

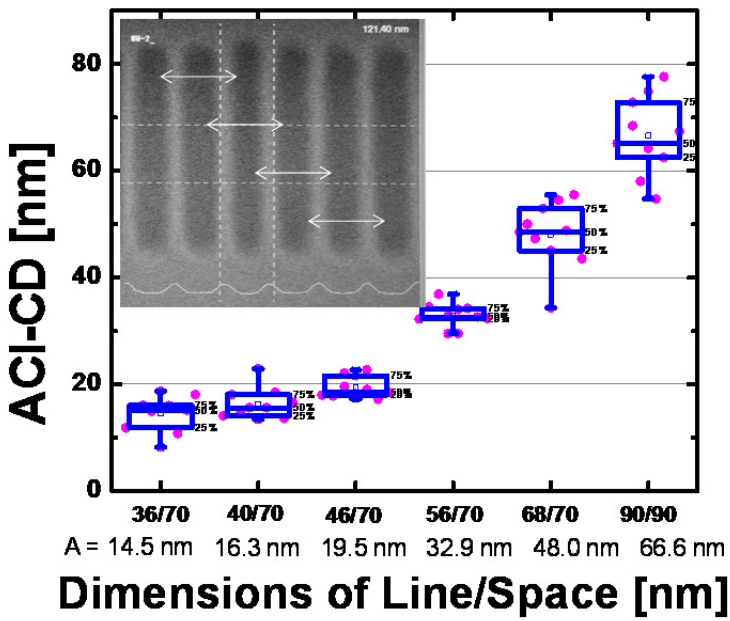
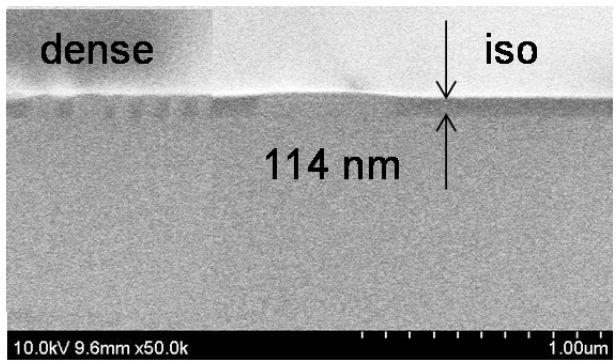


Fig. 3.2. After-cleaning-inspection (ACI) image of nanowire array.

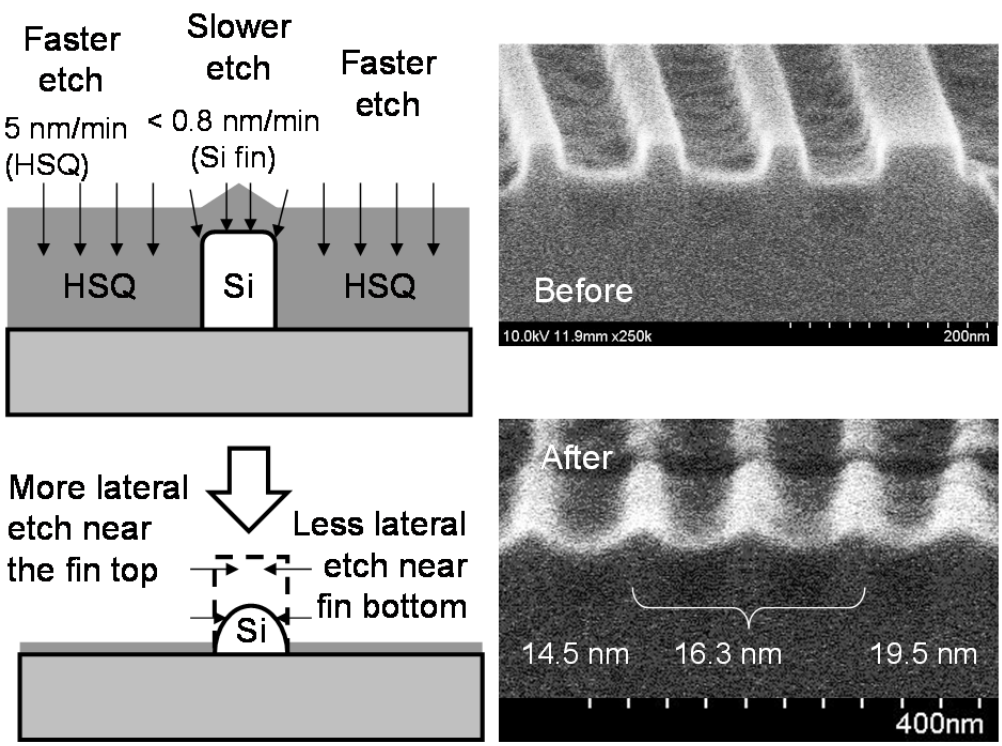
was risky because the SOI/BOX interface was not flat.

Hydrogen silsesquioxane (HSQ)-based negative EBL process for the mix-and-match lithography process was used to image nanowire patterns over the SOI wafers. By measuring the EBL/initial marker overlay errors and using them as offset values for following photolithography steps, the photolithography-to-EBL overlay errors were well-controlled within the overlay limitation of the photolithography tool or 150 nm.

Forming nanowire patterns finer than 30 nm without any additional size reduction technique is very challenging. This is because the isolated patterns and nested patterns behave in the opposite way in EBL and RIE systems. While the nested patterns usually



(a)



(b)

Fig. 3.3. Chemical corner-rounding process:
(a) after SOD planarization (HSQ), (b) rounding process by differential wet etch.

suffer from line-width thickening by charging effect and electrostatic pattern collapse in EBL systems, un-dummied isolated lines tends to thicken due to RIE loading effect in RIE systems [42, 43]. Therefore, with thinner HSQ resist and EBL dummy/spacing strategy, nanowire active with minimum W = 14.5 nm were successfully formed (Fig 3.2). More details on nanowire patterning can be found from the previous work [44].

As-etched nanowires usually have sharp corners where the unwanted field crowding occurs to degrade gate insulator reliability. Although hydrogen anneal is commonly used for the corner-rounding of nanowires, the resultant GAA structure is not a viable shape for the substrate-bias control [45]. Therefore, a new corner-rounding method based on chemical etching process was developed in this work. The idea of this method is to use the difference of etch rates between the sacrificial film and the silicon in an NH_4OH/H_2O_2/de-ionized H_2O mixture (APM). Since APM etches the sacrificial HSQ oxide six times faster than Si at a very slow rate, the top region of the nanowire fin dwells in APM longer than the bottom region of the fin (Fig. 3.3). The extent of rounding is controllable with the selection of sacrificial material and the repetition of deposition/etching cycles. As a result, this method can round the corners of Si nanowires without significant loss of the BOX layer.

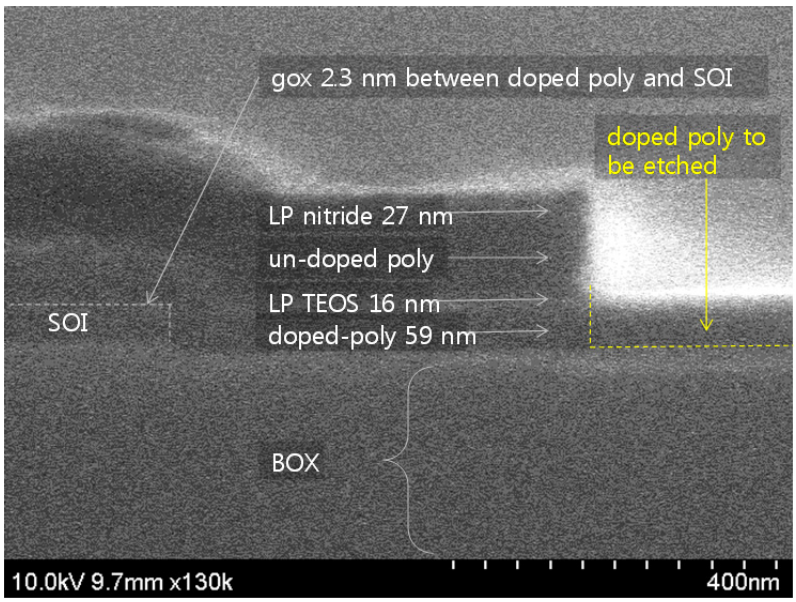
Special care had to be taken in handling wafers after the nanowire formation because the nanowires of high aspect ratio were very susceptible to pattern collapse and breakage. All the polymer and particle removal were done in a 1:8:64-diluted APM solution at 65℃ when the nanowire patterns were exposed [46, 47]. Also the rinsing after every wet

cleaning step was done with only bubbling in the overflowing bath without jet spraying. Finally, all the rinsed wafers were carefully hand-dried one-by-one with N_2 blowing to prevent any possible pattern breakage due to vibration and centrifugal force during spin drying.

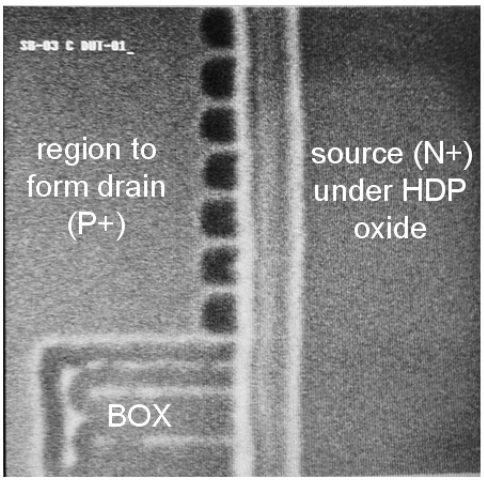
3.3 Self-aligned Formation of Gate and Asymmetric S/D Regions

Most of the previously fabricated planar TFETs have used non-self-align method to form symmetric S/D. Therefore, the minimum size of gate patterns strongly depended on the overlay error limit of the imaging tools [15, 28, 48, 49]. In this work, however, a self-aligned integration of the opposite S/D polarities was possible by sequentially forming the two sidewalls of a gate line (Fig. 3.4 and 3.5).

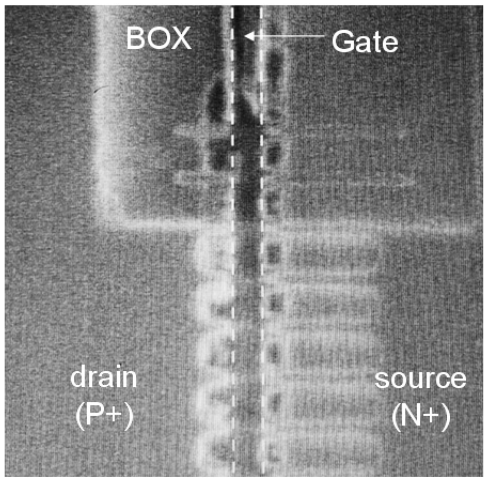
Over the nanowire-patterned substrates prepared with the sequence explained in Sec. 3.1, the gate stack of thermally-grown silicon oxide (T_{OX} = 2.3 nm) and phosphorus-doped poly-silicon (59 nm, $N_D = 4.03\times10^{20}\,cm^{-3}$) was formed. On the gate stack, the hard mask pattern of 16-nm silicon oxide / hard mask poly silicon / 27-nm silicon nitride capping was formed to cover the area for the later processes to define the other side of TFET gate and to form the TFET S/D region of the other polarity. The silicon nitride capping layer on top of the hard mask pattern was important to prevent lateral loss of hard mask poly-silicon during the gate etch process. Plasma oxidation treatment on the silicon nitride capping layer before photolithography was very effective to improve dry-etch slope of the hard mask pattern while suppressing the resist footing [50].



(a)



(b)



(c)

Fig. 3.4. Self-aligned integration scheme for asymmetric S/D:
(a) before source-side gate RIE,
(b) after drain-side gate RIE, and (c) after HDP pull back.

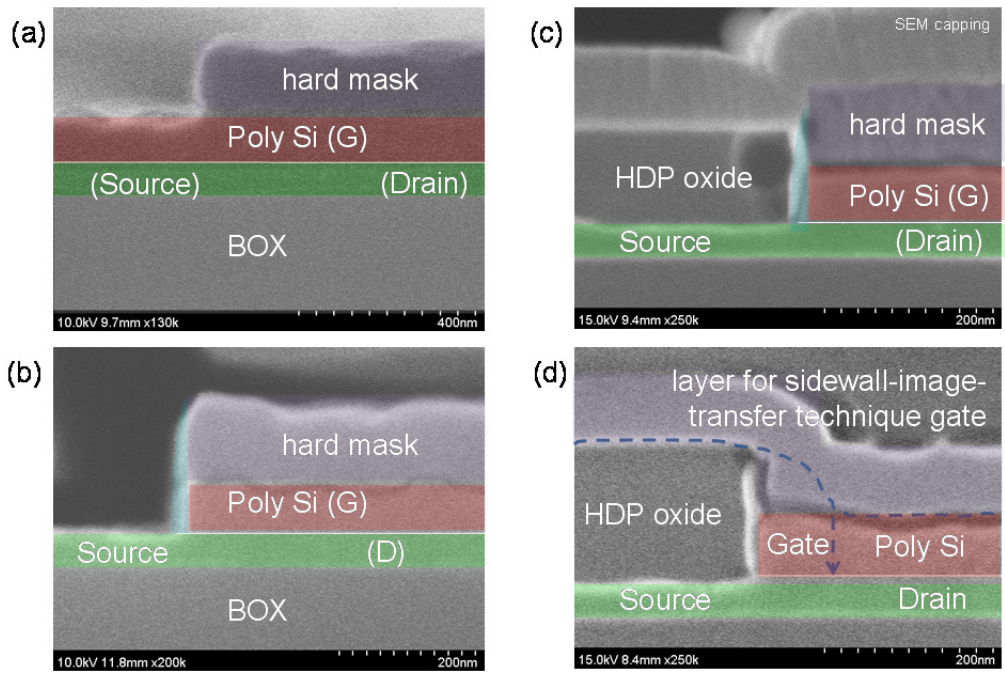


Fig. 3.5. Step-by-step cross-section images: (a) after hard mask RIE, (b) after source-side gate RIE and sidewall spacer formation, (c) just before hard mask open, and (d) just before drain-side gate RIE.

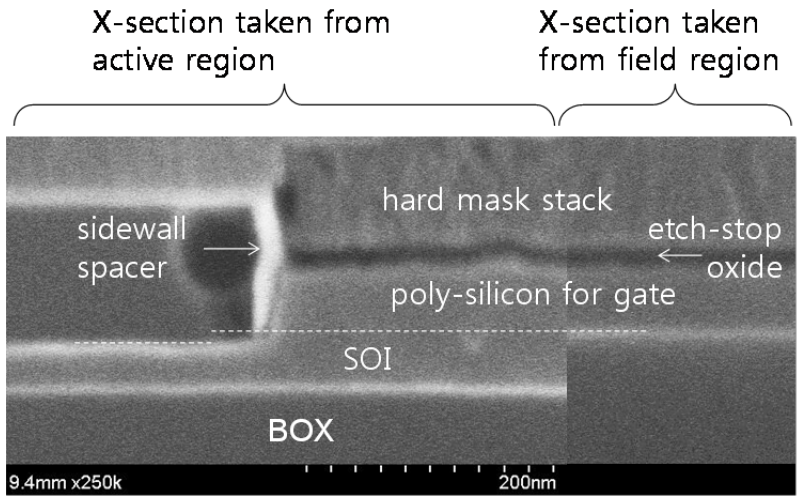
After mix-and-match process of the patterned hard mask and gate photolithography followed by oxide etch-stop strip, the poly-silicon gates for MOSFETs and one side of the gates of TFETs were etched. Since the stopping oxide was as thin as 2.3 nm, a very careful control of etch process was needed. Using Lam TCP9400DFM etcher of the NNFC, the gate poly-silicon layer was etched with a specially developed etch recipe. During the first step of the RIE recipe, the poly-silicon layer is etched with a chemistry of 100:1 silicon-to-oxide selectivity until the remaining poly-silicon becomes around 10 nm.

During the second step, the remaining poly-silicon layer was removed with a chemistry of ~10000:1 selectivity. With this special etch scheme, gate etch precisely stopped on the 2.3 nm silicon oxide while completely removing poly-silicon spacer around the nanowire patterns.

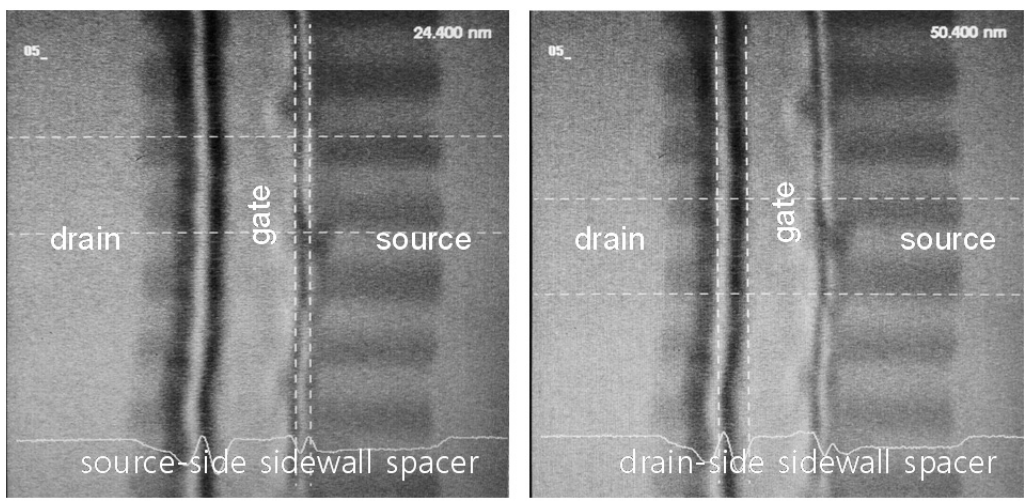
3.4 Sidewall Spacer and Self-aligned Silicide Processes

In Section 2.3, it was shown that very thin sidewall spacers were needed to improve the characteristics of TFETs. However, the improper etch stop of fluorocarbon-based RIE process was found to cause silicide formation failure [51]. Therefore, careful selection of sidewall film stack and etch control were needed. For the source-side sidewall spacer, 17 nm of LPCVD silicon nitride over 8 nm of LPCVD oxide was deposited and etched back in a magnetically-enhanced RIE system (P-5000, Applied Materials Inc.) with a $CHF_3/CF_4/Ar$ chemistry. Diluted APM treatment was needed to clean up the volatile by-product after etch process. The amount of etch was determined lest the micro-trenching profile should consume the active silicon more than 10 nm. The drain-side sidewall spacer was formed to be ~ 45 nm with 12 nm of LPCVD oxide and 35 nm of LPCVD nitride to suppress unwanted tunneling current at the channel/drain boundary at off-state. Final images of the sidewall spacers and RIE control are shown in Fig 3.6.

Self-aligned nickel silicide was formed with proper pre-metal surface treatments and two-step anneal scheme. Since the previous study clearly showed that the control of the carbonated silicon surface was critical to the successful formation of SALICIDE, the



(a)



(b)

Fig. 3.5. Images of sidewall spacer:
(a) RIE control and (b) final images of sidewall spacers of different lengths.

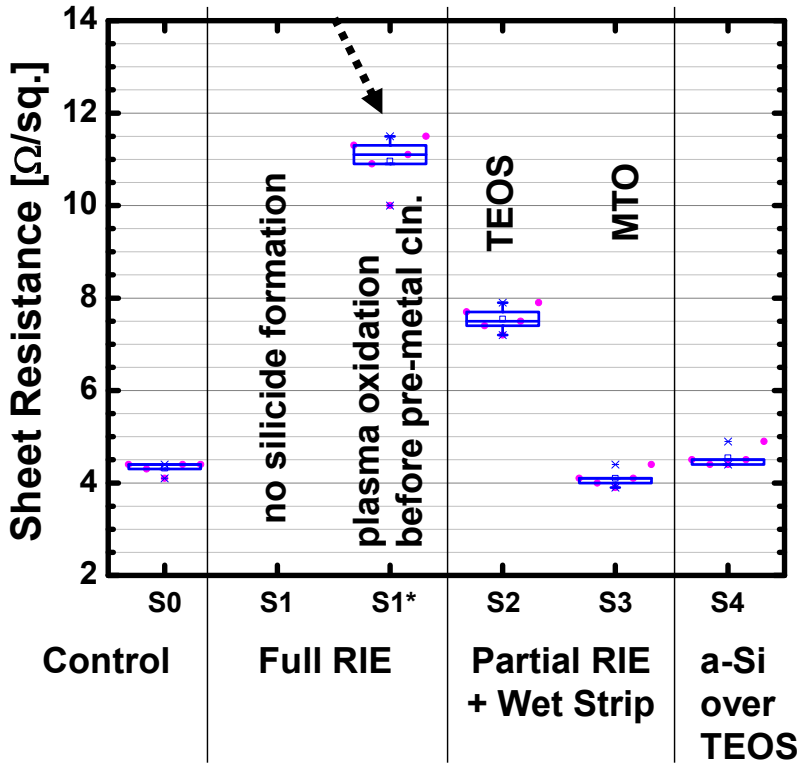


Fig. 3.6. Preliminary test to optimize the pre-silicide treatment process [16].

wafers were treated with the oxygen plasma and diluted APM, and proceeded to pre-nickel HF cleaning (Fig. 3.7) [51]. For the pre-nickel HF cleaning, a diluted (100:1 by volume) mixture of HF (49% electronic grade) was used. TEM-calibrated 10 nm of pure nickel film was deposited immediately after the pre-nickel HF cleaning. After selectively forming the initial silicide on the exposed silicon region at 270℃, the remaining un-reacted nickel over dielectric materials was selectively removed in a H_2SO_4/H_2O_2 mixture solution (SPM) at 80℃. Additional annealing at 450℃ after the selective metal strip was

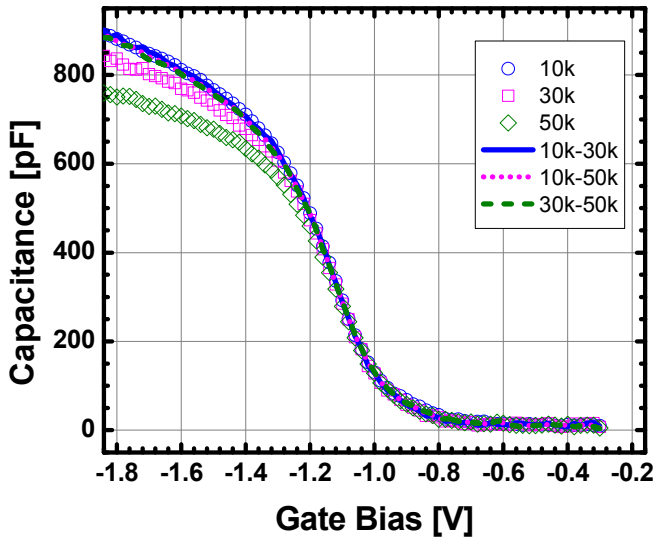
performed to transform the initial silicide to lower resistance phase [52, 53]. Successful formation of the low resistance silicide was confirmed from the four-point resistor patterns co-integrated with the TFETs and MOSFETs.

Chapter 4

Device Characteristics

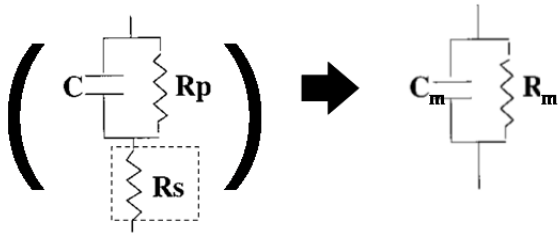
4.1 Fabricated Metal-Oxide-Semiconductor Capacitor

As shown in Chapter 2, the gate oxide thickness is one of the most important factors that influences both the switching characteristics and current drivability of TFETs. Therefore, the quality of the gate oxide was characterized with the bulk wafer used to monitor the gate stack processes of the main wafers. The physical oxide thickness the right after the growth was 2.3 nm in average and the difference between the maximum and minimum values was 0.4 nm from the 9-point measurement with a TEM-calibrated ellipsometer. The metal-oxide-semiconductor capacitors with the area of 300 μm × 300 μm were fabricated with the monitoring wafer and other two reference wafers of 4- and 10-nm thermal oxides. The capacitance-voltage (*C*-*V*) characteristics of the 2.3 nm capacitor samples measured with Keithley 4200-CVU system showed the frequency dispersion behavior, while those of thicker-oxide samples did not (Fig 4.1). In order to remove the dispersion component to obtain true capacitance value, Yang and



(a)

$$Z = R_s + [(j\omega C)^{-1} \parallel R_p] \quad \Rightarrow \quad Z = [(j\omega C_m)^{-1} \parallel R_m]$$



$$C = \frac{{f_1}^2 C_{m,1}\left(1 + {D_1}^2\right) - {f_2}^2 C_{m,2}\left(1 + {D_2}^2\right)}{{f_1}^2 - {f_2}^2}$$

, where $D_1 = \left(\omega_1 \, R_{m,1} \, C_{m,1}\right)^{-1}$

(b)

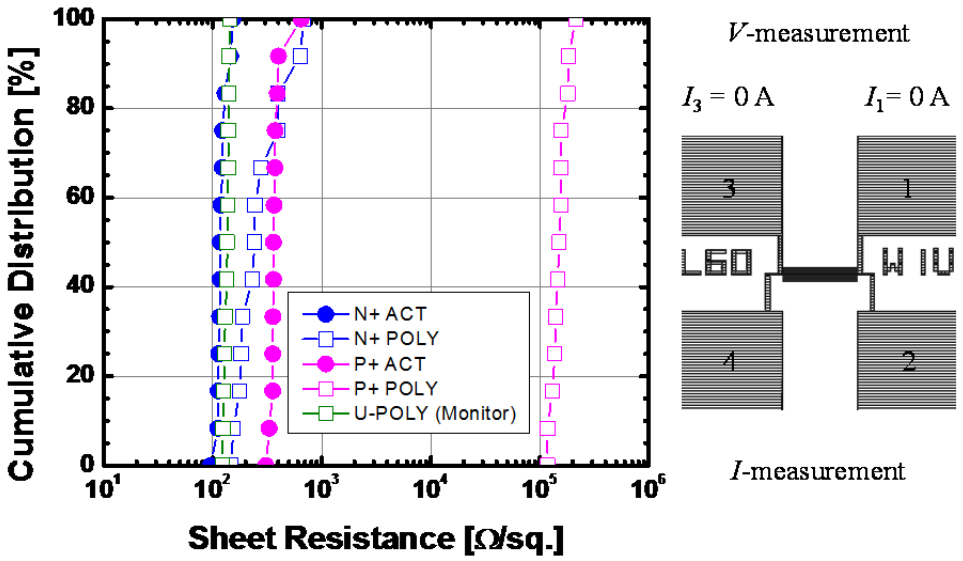
Fig. 4.1. Frequency compensation of the *C-V* curves from the monitoring MOSCAP: (a) measured *C-V* curves and (b) theory [19].

Hu's multi-frequency method was tried with three different frequencies [54]. As a result, all the compensated *C-V* curves met on one curve. From the converged compensated curves, the equivalent oxide thickness (EOT) was extracted with CVC program of North Carolina State University [55]. With consideration of quantum effect and poly depletion, the extracted equivalent oxide thickness was 2.84 nm in average and the difference between the maximum and minimum values of the measured data was 0.28 nm.

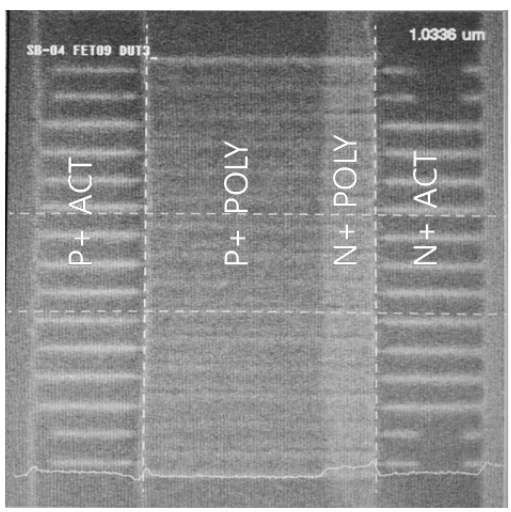
From these results, it was confirmed that sub-3 nm EOT was achieved on the main wafers. However, it was also found that the gate leakage is so significant that it requires a careful consideration to analyze the transistor measurement data.

4.2 Junction Properties of Co-Integrated MOSFETs

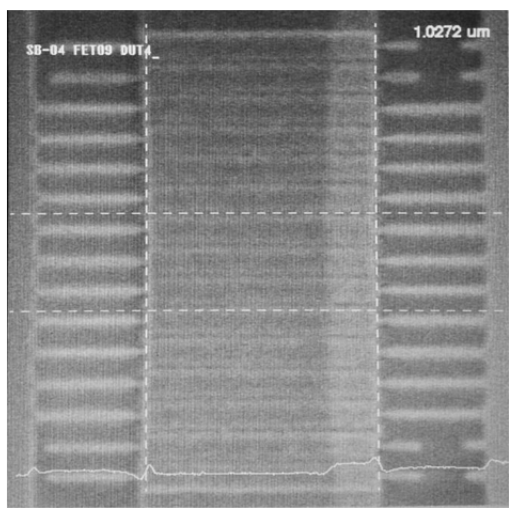
Since the snowploughing effect during silicidation was planned to form the abrupt dopant profile, the formation of silicide was examined first. The semiconductor parameter tester, Agilent 4156C, was used to obtain *I-V* characteristics after official calibration at manufacturer's site. By comparing the resistance values of the four-point resistors with those of the un-doped resistors in the monitor wafer and studying linearity of I_{24}-V_{13} curves, it was confirmed that the silicides were successfully formed on n^+ and p^+ active regions and n^+ poly region (Fig. 4.2). The poly resistors with p-type ion implantation showed very high resistance ($\times 10^5$ Ω/sq.) and the region appeared with darker contrast than the other silicided regions in the in-line inspection SEM images. Since the phosphorus-doped poly-silicon was used in this work, the poly-silicon patterns



(a)



(b) TFET with W = 16 nm



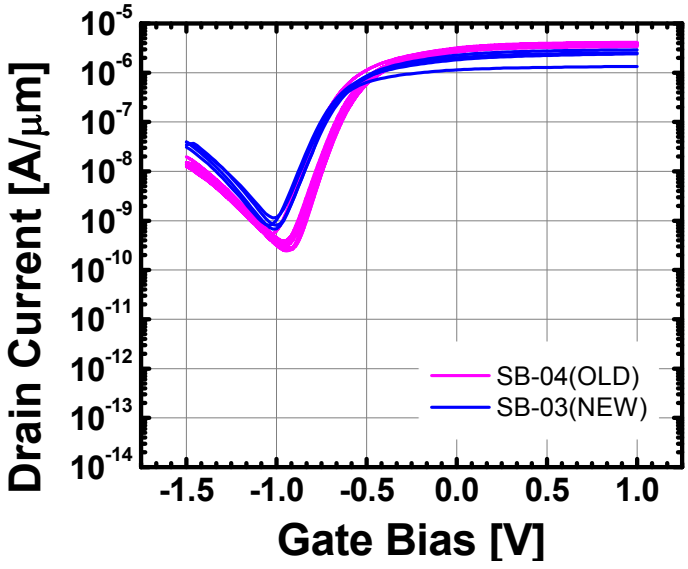
(c) TFET with W = 33 nm

Fig. 4.2. Resistance of four-point resistors after SALICIDE and inspection SEM images of silicide on TFETs: (a) resistance data, and (b) and (c) TFET images.

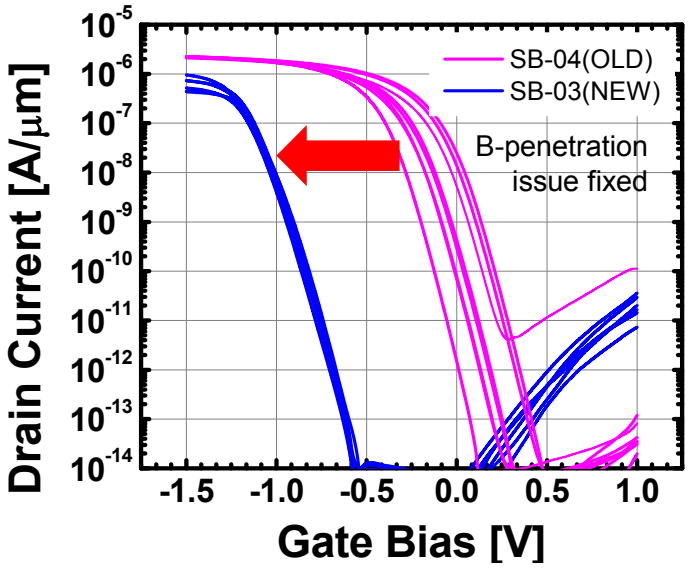
with p-type ion implantation actually had dopants of both polarities in high concentrations [56]. This is assumed to be the cause that the silicide formation was inhibited.

In order to understand the electrical properties at the n-type and p-type boundaries, the co-integrated n- and p-channel MOSFETs were studied. Figure 4.3 shows the transfer characteristics of long-channel MOSFETs with L = 1 μm, W = 10 μm, and T_{body} = 55 nm. The V_T of n-channel devices is negative and the devices operate as depletion-mode device. Such negative V_T appears typically with the ultrathin-body devices due to their small depletion charge. The gate-induce drain leakage (GIDL) current of the n-channel devices is noticeably strong. This may be because the snowploughing effect had the dopant profile abruptly change around the silicide edge. Meanwhile, the p-channel devices show much smaller GIDL current, implying that the p-type dopant profile is less abrupt at the p-type region boundary. From these results, the fabricated junctions are thought to be more suitable for the p-channel device operation than the n-channel mode operation.

The p-channel MOSFET with an optimized ion implantation and activation anneal conditions shows very high $|V_T|$ values of very tight distributions. It was understood that the in-situ doping of phosphorus-doped poly-silicon was so heavy ($N_D = 4.03\times10^{20}$ cm^{-3}; PSD) that the p-type source/drain ion implantation (BF_2 10 keV 2×10^{14} cm^{-2}) could not have a significantly influence on the device characteristics. It was re-verified from TCAD simulation also. The p-channel devices with non-optimized doping condition



(a)



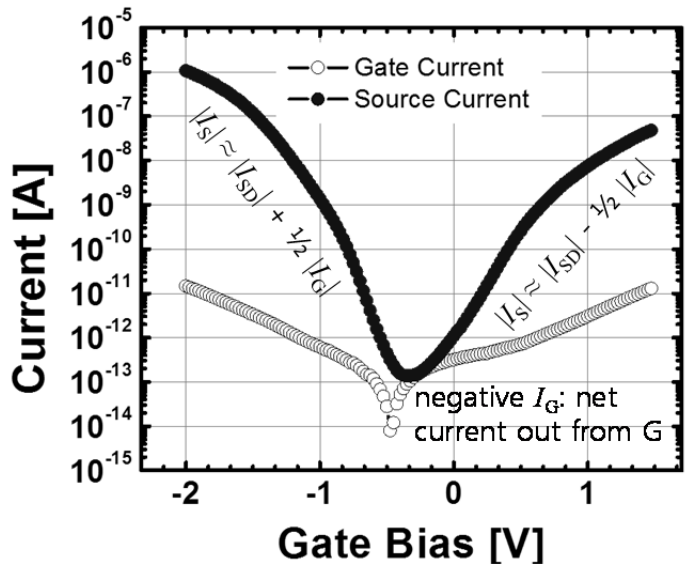
(b)

Fig. 4.3. Subthreshold transfer characteristics of n- and p-channel MOSFETs: (a) NMOSFET and (b) PMOSFET. Here L =1 and $|V_{DS}|$ = 0.1 V. Here the old/new PSD doses are 1×10^{15} cm^{-2} and 2×10^{14} cm^{-2} respectively. The activation conditions are 1000℃ 3 s and 900℃ 10 s for old and new ones respectively.

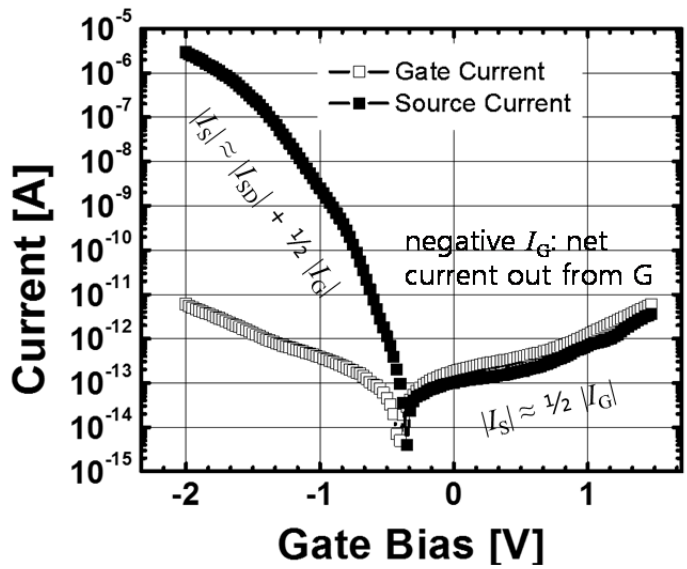
(BF_2 10 keV 1×10^{15} cm^{-2}) showed much lower $|V_T|$ with a severe variation. Considering that the subthreshold swings remained unchanged and the sign of V_T was still negative, boron penetration influenced the variation of the devices in the un-optimized case.

4.3 Transfer and Output Characteristics of TFETs

First, in order to make proper interpretation of the measured results, the transfer characteristics of long-channel TFET (L = 1 μm) fabricated with the non-self-align method were examined (Fig. 4.4). The gate leakage current was quite significant so that a special care was needed in evaluating the switching characteristics. Since all the currents (I_G, I_S and I_D) are measured at the terminals of the tester, the true current between the source and drain modulated by the gate (I_{SD}) is difficult to be exactly measured. For example as shown in Fig. 4.5, the off-state drain current ($V_G = V_S = 0$ V and $V_D = V_{OP}$) is composed of the currents from the gate and the source while the measured on-state drain current appear as the net current with consideration of I_{SD} and a current going out to the gate. At the on-state, I_{SD} is so large that the current loss to the gate is insignificant. However, if the device is near off-state and I_{SD} is extremely small, I_D is almost equal to the current from the gate. On the contrary, the current flowing out to the gate from the source is negligible if the device is near off-state. In addition, the source current flowing out to the gate at the on-state gate bias (V_{OP}) is negligible compared with I_{SD}. Therefore, we can assume that I_S is close to I_{SD} for all gate biases. As V_G goes beyond the off-state condition, the gate leakage also starts to increases. This



(a)



(b)

Fig. 4.4. Current measured from the source and gate terminals: (a) device with optimized p^+ condition and (b) device with the penetrated boron in the channel. Here L =1 μm, W = 33 nm × 11, and V_{DS} = -0.1 V.

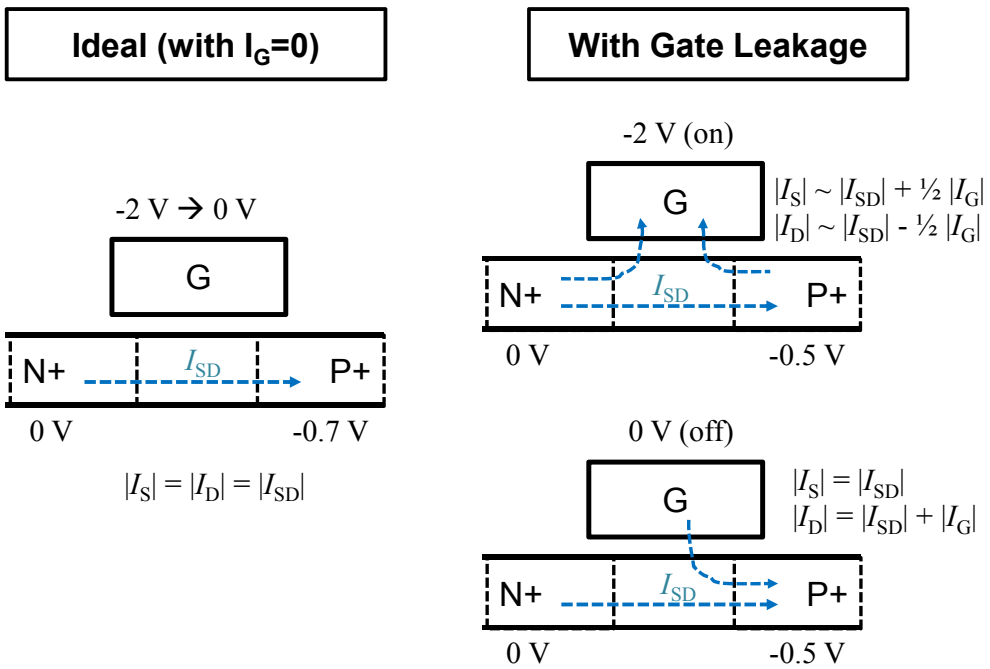


Fig. 4.5. Model to understand the best measurement method.

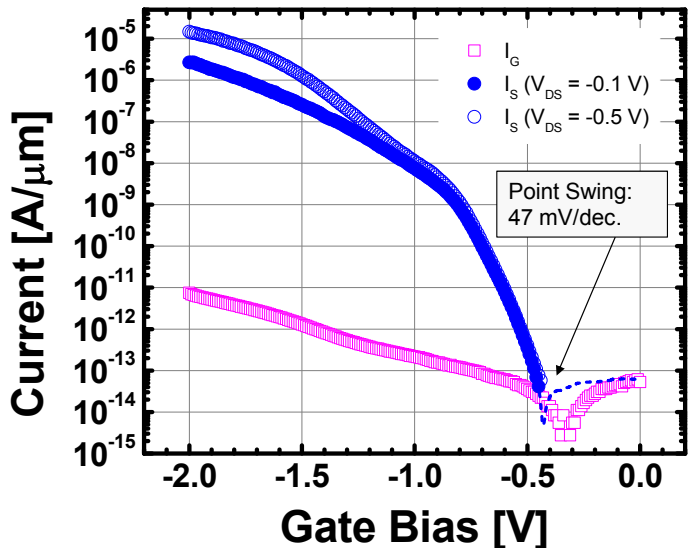
will cause sign changes in I_G and I_D as V_G increases. Especially this becomes an important issue when one should decide whether a measurement value is trustworthy or not. Therefore, in this work, I_S was selected as a monitor parameter to study the transfer characteristics of the device. In order to extract the minimum swing from $\log_{10}(I_S)$ vs. V_{GS} plot, a small bias of –0.1 V was applied to the drain. All the I_S values smaller than 1×10^{-14} A or half of I_G were ignored. The I_S values with $I_G > 0$ were also ignored because it is the indication that the current may start to flow toward the source terminal. After the point showing minimum swing was determined, V_{OFF} was defined as the V_G at the point and V_{ON} as $V_{OFF} + V_{OP}$. With the definition of V_{ON} and V_{OFF}, I_{ON}, I_{OFF} and their

ratio were obtained with $V_{DS} = V_{OP}$. Here V_{OP} was set to be -0.5 V.

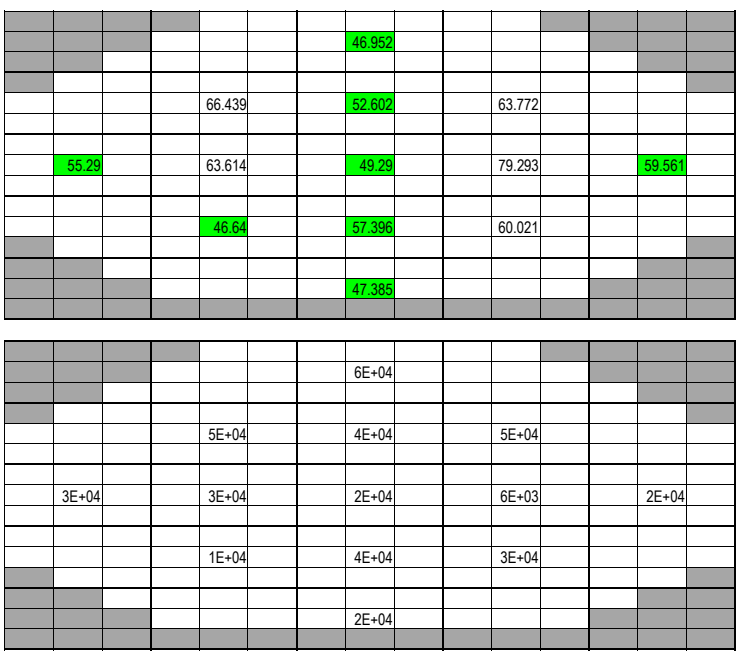
Figure 4.6 shows the subthreshold transfer characteristics and the wafer maps of minimum point swing and I_{ON}/I_{OFF} from the fabricated Si nanowire long-channel TFETs (L = 1 μm, W = 32.9 nm × 11). The device structure was designed to have 11 devices connected in parallel to make best use of the resolution limit of the tester. The best point swing from the measured devices was 47 mV/decade. The I_{ON}/I_{OFF} ranges from 1×10^4 to 6×10^4 with one maverick point of 6×10^3.

Figure 4.7 is the output characteristics of the long-channel TFET with the best performance. The current saturation behavior is very similar to TCAD simulation shown in Chapter 2. The I_D slowly increases with V_{DS} until it reaches the saturation value at a quite high V_{DS}.

In the following sections, how the device characteristics actually change with design parameters is to be shown.

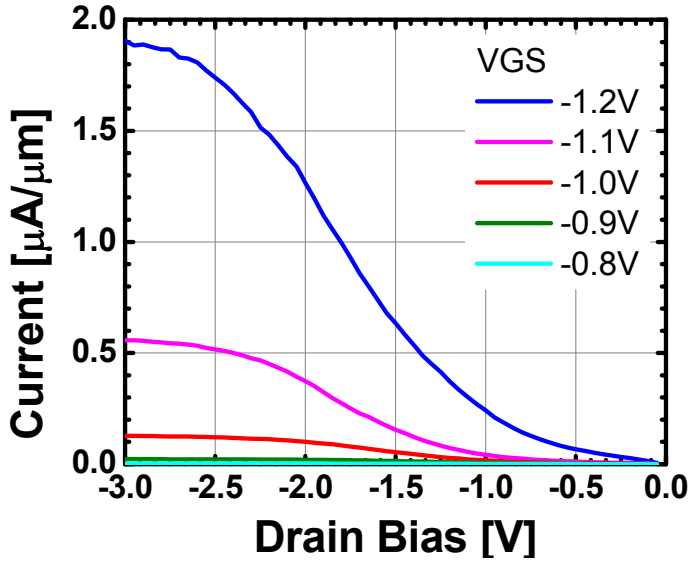


(a)

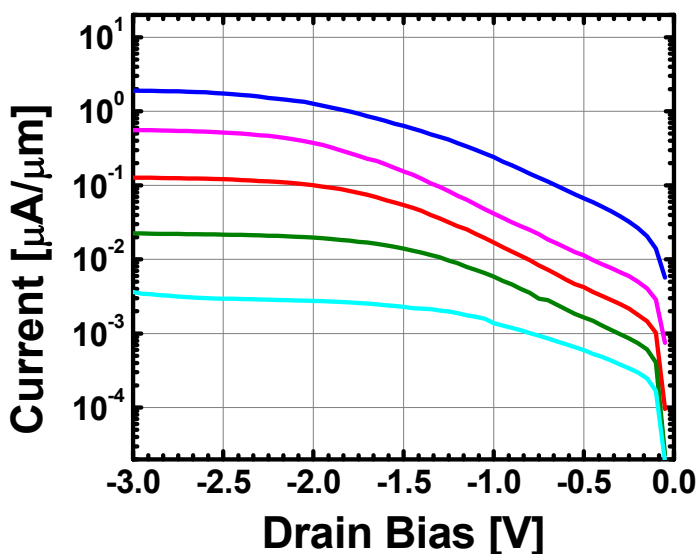


(b)

Fig. 4.6. Transfer characteristics of the long-channel TFETs: (a) I_S-V_{GS} and (b) wafer maps. Here L =1 μm, and W = 33 nm × 11.



(a)



(b)

Fig. 4.7. Output characteristics of the long-channel TFET:
(a) linear scale plot and (b) log scale plot. Here L =1 μm and W = 33 nm × 11.

4.4 Device Properties with Design Partitioning

4.4.1 Active Width

Figure 4.8 shows the change of transfer characteristics with the active dimension. Although the successful formation of the nanowires as thin as 14.5 nm in width were confirmed from in-line inspection, the number of electrically working nanowire devices drastically decreased as W decreased below 33 nm. With the measured set of devices though, the current drivability is seen to increase as W decreases. As studied from Chapter 2, this is thought to be due to the enhanced geometric and field coupling effects.

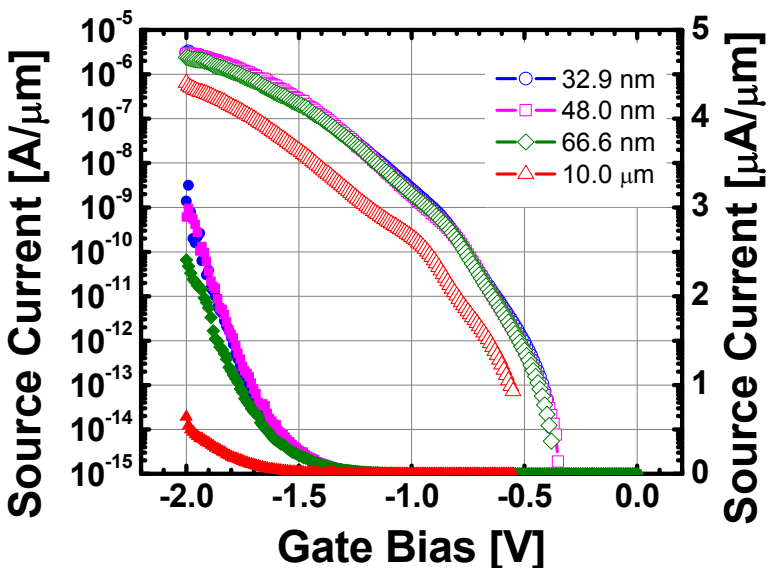


Fig. 4.8. Change of transfer characteristics with the active width
Here L =1 μm, V_{DS} = -0.1 V, and 11 transistors are connected in parallel.

4.4.2 Channel Length

Thanks to the advanced self-aligned integration scheme for the asymmetric S/D, the TFETs of very small channel lengths were successfully integrated. However, due to the non-uniformity of the planarization process, the number of working devices significantly decreased (Fig. 4.9). Gradual degradation of slope of $\log_{10}(I_S)$ vs. V_{GS} curves with the gate length is seen in Fig. 4.10. In order to see the trend more clearly, more devices were measured and the minimum point swing values were extracted. When plotted with the gate length measure in inspection SEM, the point swing showed the indication of short-channel effect (Fig. 4.11). Since most of the previous fabricated TFETs were long-channel devices with $L \geq 0.25$ μm, the short-channel effect of TFETs has not been seriously considered. However, this result experimentally shows that the short-channel effect is also important in scaling-down of TFETs and a careful device design to prevent this phenomenon is needed. By reducing W down to 19.5 nm, it is found that a short-channel device with L = 109 nm can be improved (Fig.4.12).

In order to understand more on the short channel effect of TFETs, TCAD simulations of nanowire devices are added. For this study, two different cases of channel doping are considered; n- and p-type channels. With a low doping level of 10^{15} cm^{-3}, the polarity of the channel do not make any difference in the transfer characteristics for various L's. However a significant difference occurs in the case with $N = 10^{18}$ cm^{-3} (Fig. 4.13). The case that the channel polarity is the same as that of the drain region is already studied in Chapter 2. As L decreases, the drain potential starts to influence the tunneling

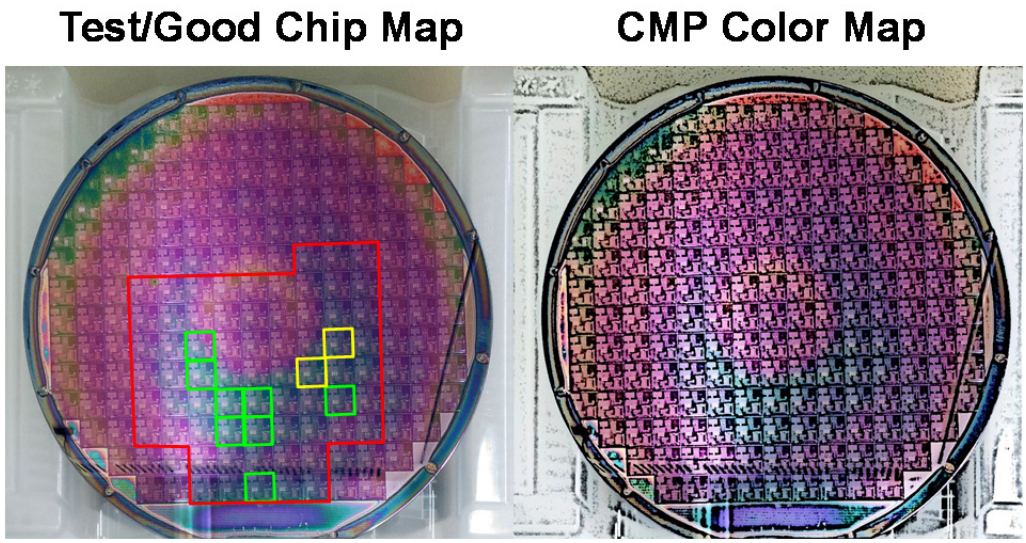


Fig. 4.9. Locations of working short-channel devices and wafer coloring after CMP.

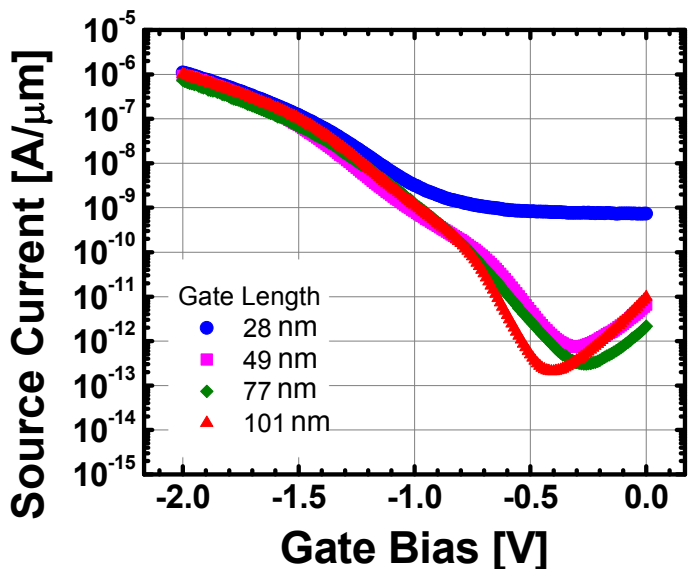
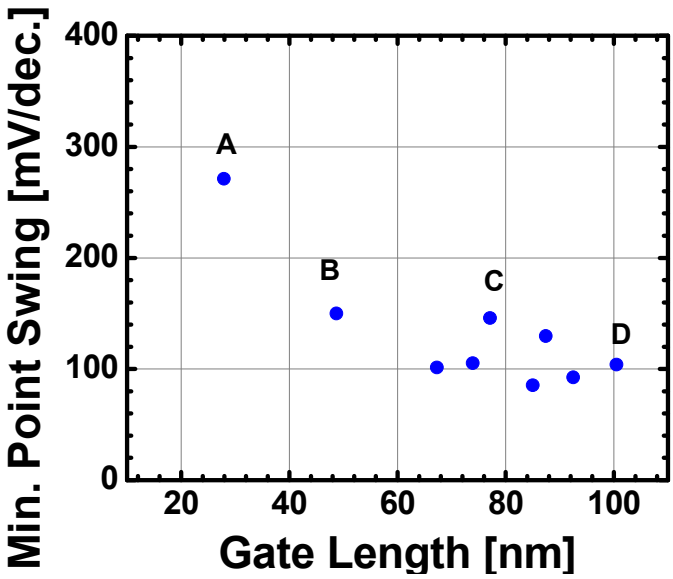
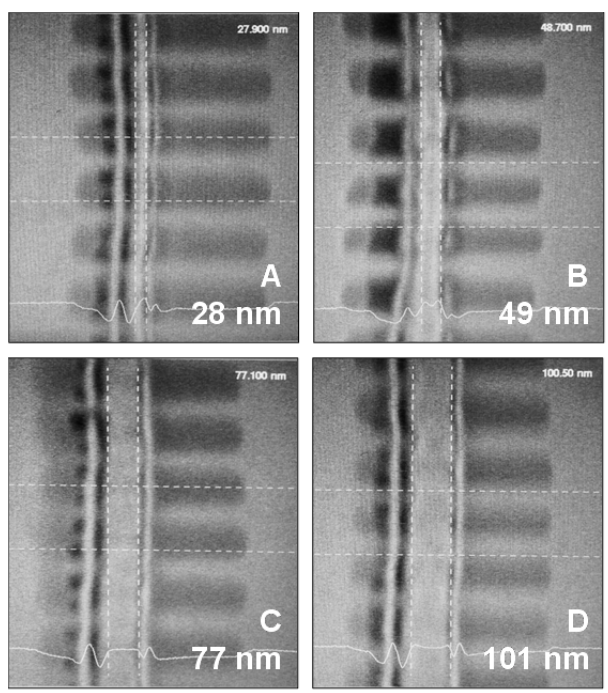


Fig. 4.10. Change of transfer characteristics with gate length:
Here W =33 nm × 31 and V_{DS} = –0.1 V.



(a)



(b)

Fig. 4.11. Point swing roll-up of the short-channel TFETs:
(a) minimum point swing vs. gate length and (b) inspection SEM images.

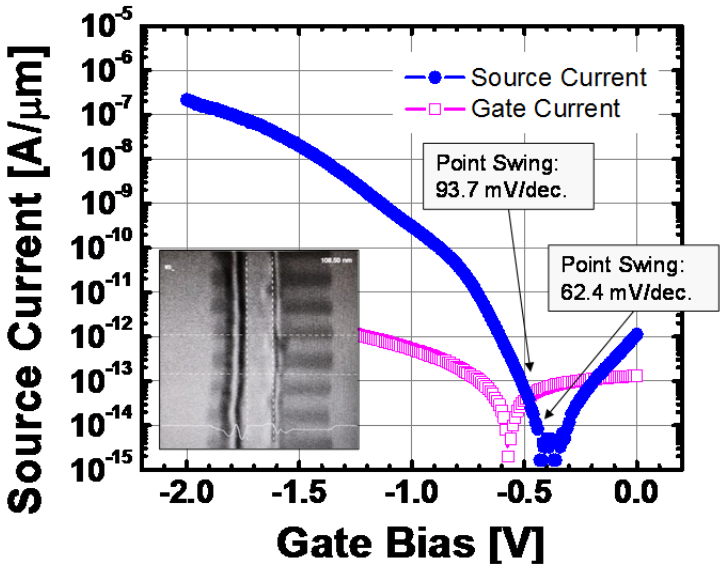
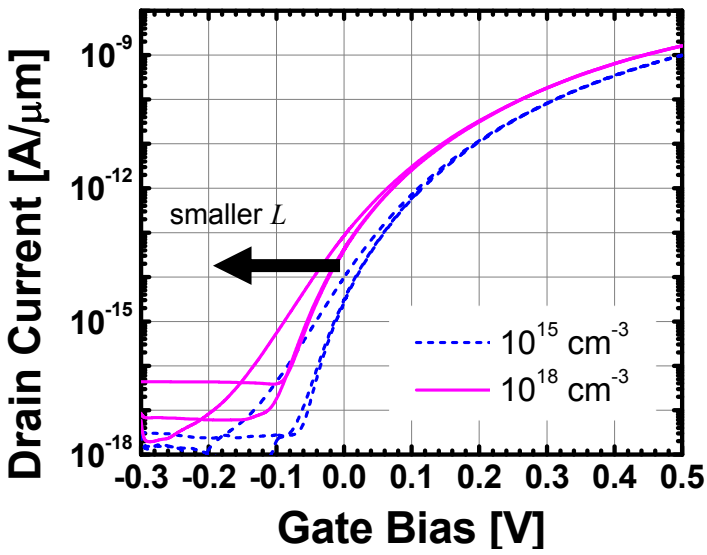
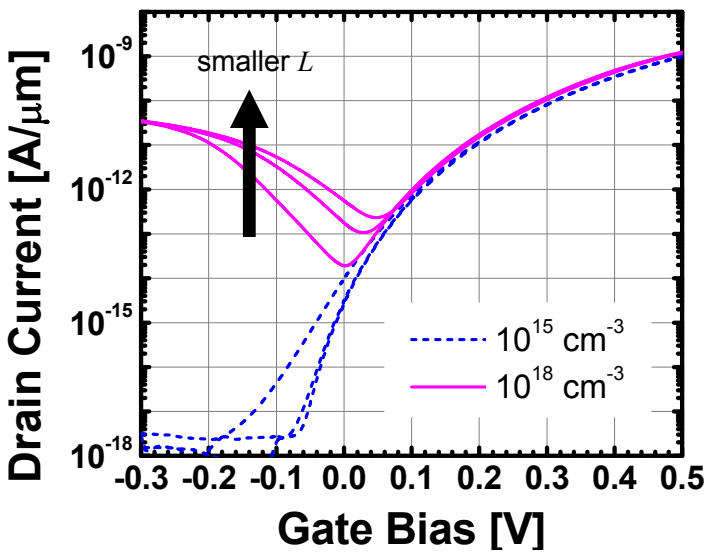


Fig. 4.12. Transfer characteristics of the best short-channel device
Here L =109 nm, W =19.5 nm × 31 and V_{DS} = -0.1 V.

barrier at the source/channel junction to increase the leakage current. The ambipolar action of the drain/channel junction is suppressed due to the small built-in potential in the region. Therefore the governing mechanism on the short-channel effect is DICE or DIBT as explained previously. In case that the polarity of the channel is the same as that of the source region, however, the prevailing mechanism is different. As L becomes smaller, the ambipolar tunneling near drain/channel junction becomes stronger due to the increased influence of the source potential on the tunneling barrier across the channel/drain junction. This also increases the leakage current with L scaling. This explains the change of $|d\log_{10}(I_{\text{ambipolar}})/dV_{\text{GS}}|$ with L in Fig 4.10. After all, the



(a)



(b)

Fig. 4.13. Short-channel effects with the channel doping:

(a) n-type channel and (b) p-type channel:

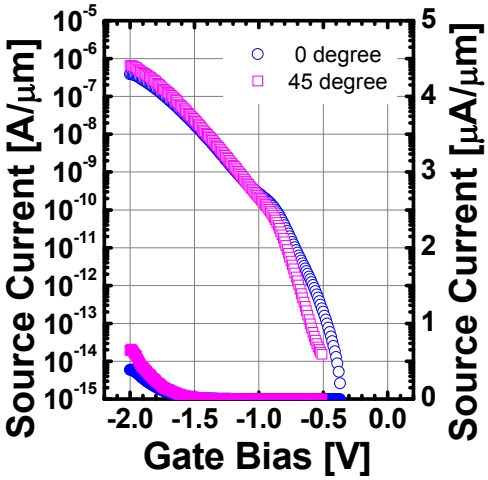
Here L of each curve is 130, 22, and 14 nm respectively, and V_{DS} = 0.5 V.

short-channel effect appears regardless of the polarity of the channel region.

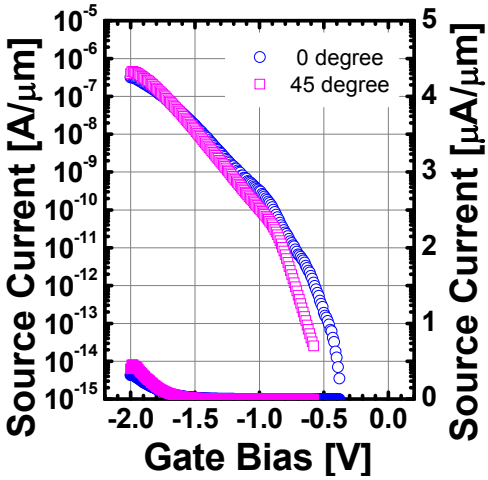
4.4.3 Channel Direction

As another device design parameter to improve the tunneling current, the effect of channel direction on (100) wafer was studied. Although TFETs are not mobility-driven devices, the tunneling rate may change with the channel direction due to asymmetry of tunneling mass and degeneracy [57]. In order to verify the idea, the devices with the channel direction tilted by 45 degree <100> to the normal direction <110> were co-integrated. Figure 4.14 shows that the <100>-channel TFET is superior to the <110>-channel TFET in terms of the current drivability and point swing in the planar system. Considering that TFETs are not mobility-driven device and the <110>-direction hole mobility is larger than the <100>-direction mobility on the (100) wafer, the observed difference is not due to difference of anisotropy of hole mobility [58]. More possible explanation of this phenomenon may be the anisotropy of tunneling coefficient, which is determined by the tunneling mass and degeneracy [37, 59]. Although the details of the results are not fully understood with the limited set of experiments, this is an important observation in that it suggest a new possibility to improve TFETs with simple change of device design or well-developed various strain techniques.

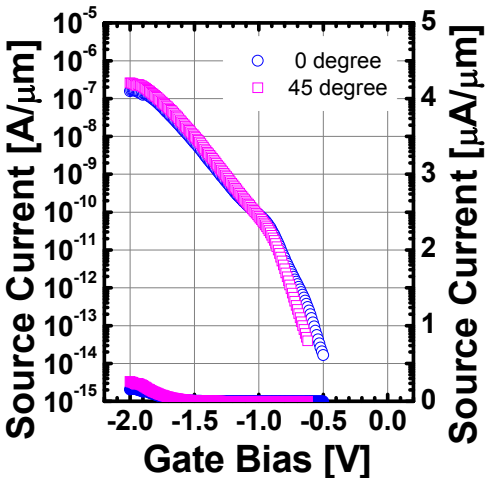
This effect was also examined with the nanowire devices but the result was difficult to interpret due to the difference of oxide growth rate on the side of the fins and the change of the strain effect by silicide (Fig. 4.15). In order to understand the results



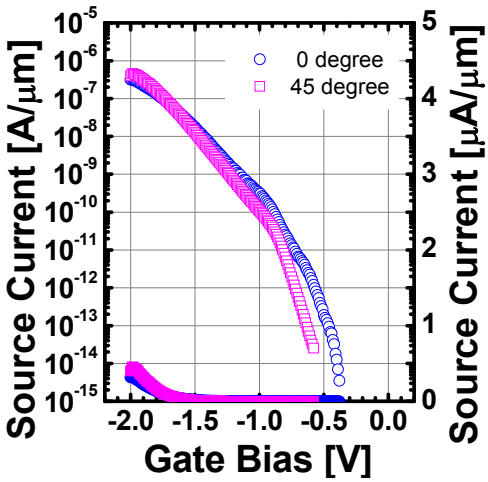
(a) Chip #1-1



(b) Chip #1-2

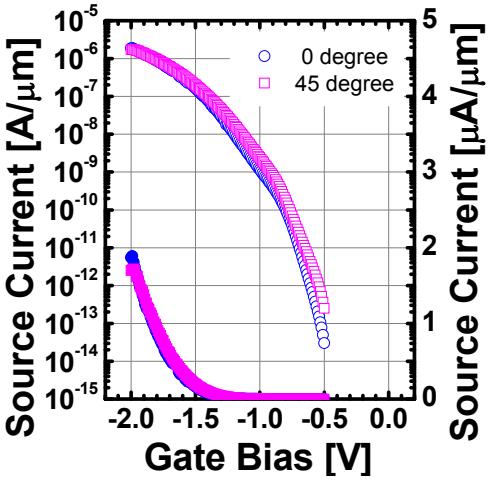


(c) Chip #1-3

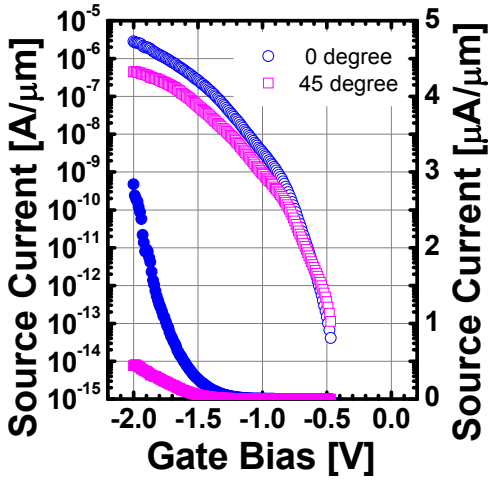


(d) Chip #1-4

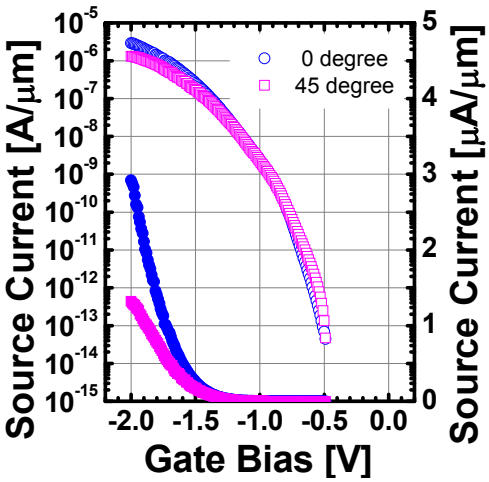
Fig. 4.14. Change of transfer characteristics of planar TFETs with the channel direction: Here L =1 μm, W =10 μm, V_{DS} = -0.1 V, and the chips were randomly selected.



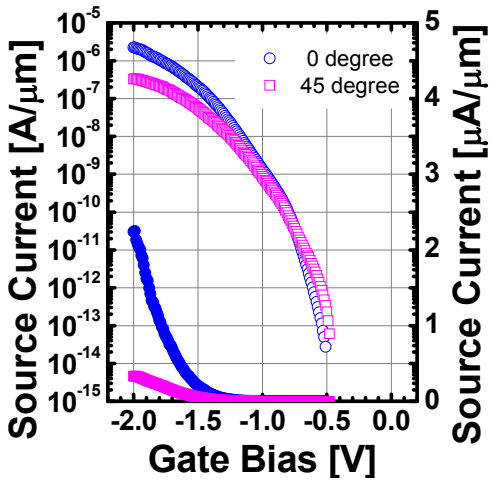
(a) Chip #2-1



(b) Chip #2-2

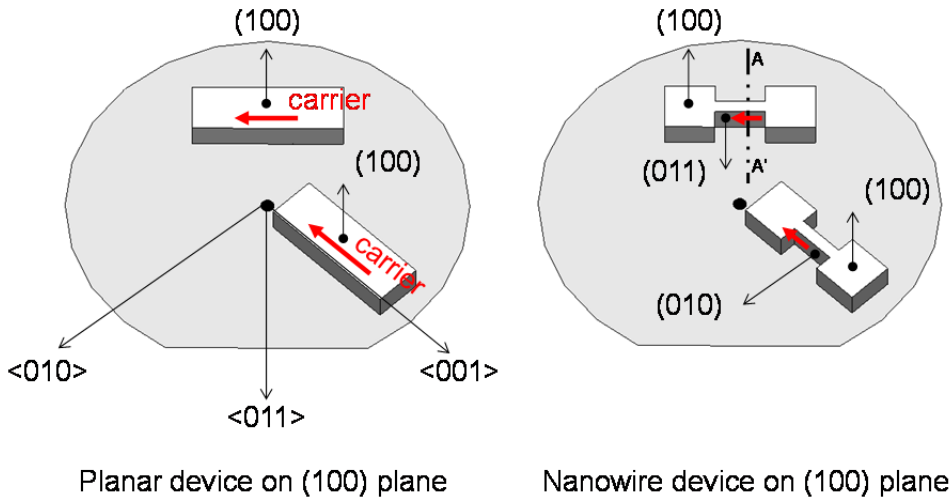


(c) Chip #2-3

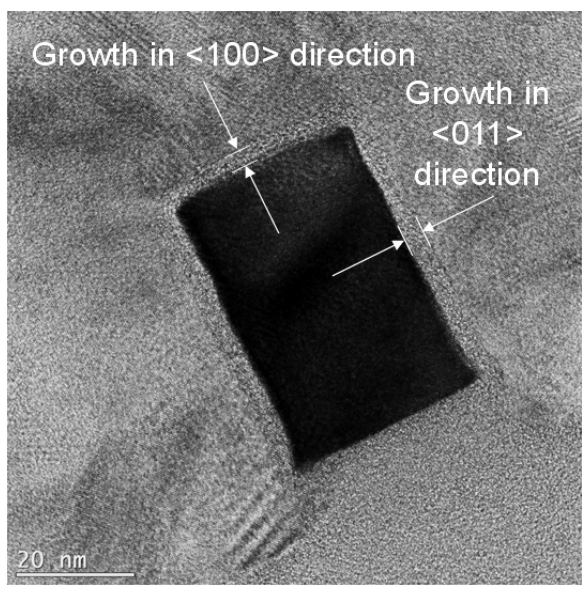


(d) Chip #2-4

Fig. 4.15. Change of transfer characteristics of nanowire TFETs with the channel direction: Here L =1 μm, W =33 nm × 11, and V_{DS} = -0.1 V.



(a)



(b)

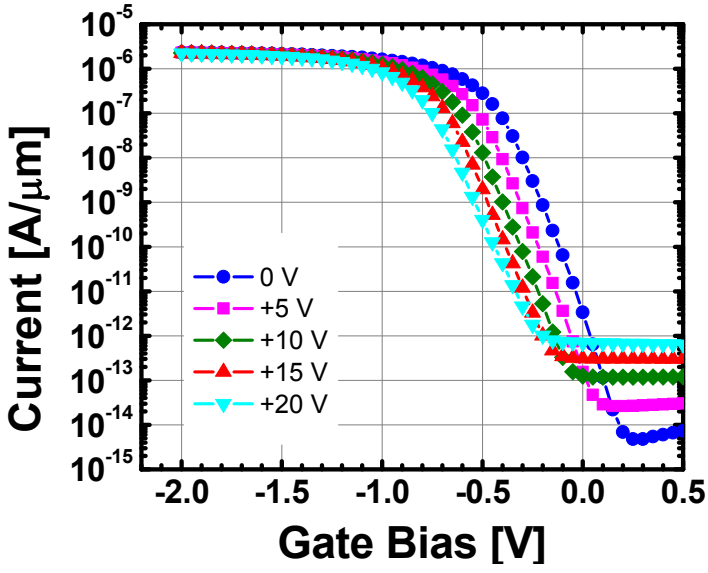
Fig. 4.16. Model to understand the variation of the planes on nanowire surfaces and transmission electron microscopic (TEM) image of the nanowire with 0-degree rotation: (a) crystal orientations and (b) TEM images across AA'.

of the nanowire devices, model nanowire devices without corner-rounding are considered in Fig. 4.16. Unlike the planar device, the nanowire device contains various surface planes. The oxidation rates of those plane is largest on (110), and (111) is the next, and the (100) is the slowest plane [60]. The TEM image also shows that the growth of gate oxide was faster on the side of 0 degree nanowire. Therefore it does not make sense to explain why the 0-degree devices outperform 45-degree devices. Another point to look is that the plane where the tunneling process occurs. While the surface plane of the planar devices are fixed to be the (100) plane, the planes on nanowires are much more complicated. Since the effective mass of carriers is determined by the crystallographic structure and orientation, this may give more clues to the difference of planar and nanowire systems. More study is ongoing to understand the results of the anisotropy experiments.

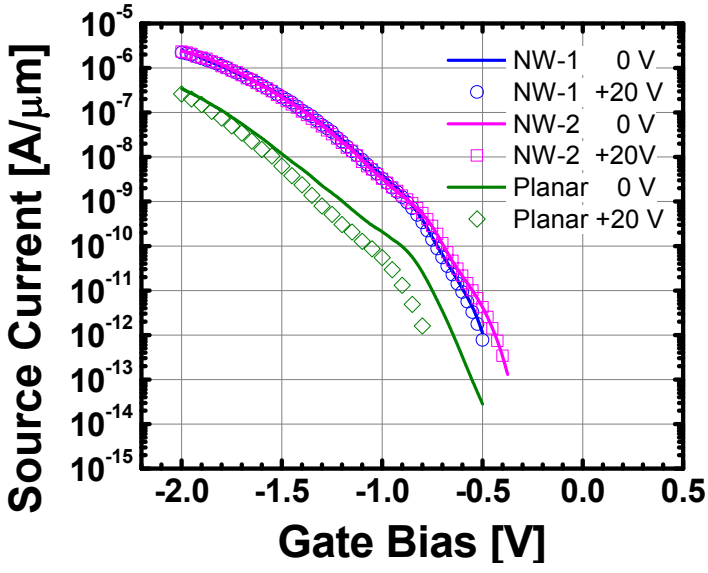
4.4.4 Back-Gate Effect

One of the important low-power CMOS design techniques is to use substrate-bias to modulate the turn-on point of MOSFETs [2]. Whether the similar technique would be applicable to the fabricated nanowire TFETs or not was studied after forming the back-gate terminal with the silver paste. The MOSFETs and TFETs in the same chip were compared with the substrate bias varied up to 20 V. Since the T_{BOX} was 375 nm, the electric field built across BOX should be similar to the case of applying 270 mV to the substrate of ultrathin-body and BOX SOI (UTBB-SOI) wafer with T_{BOX} = 5 nm. Here the

assumption is the BOX layer is very clean and the permittivity of BOX (κ_{BOX}) is close to 3.9. Figure 4.17 comparatively shows the substrate-bias tunability of MOSFETs and TFETs. While the planar MOSFET shows a shift of ~300 mV with V_B = +20 V, the planar TFET shows a much smaller change. This is because the current flow mechanism of a TFET is much stronger function of electric field than that of a MOSFET. Until the back-gate forms very high field, the tunneling current does not change. This was also confirmed from the previous TCAD simulation study on UTBB-SOI TFET [61]. The nanowire TFET showed no change of the characteristics. This is believed due to the surrounding gate are more tightly controlling the channel potential and there is almost no room for the field from the back-gate to influence the channel potential. This result indicates that the nanowire TFETs are very difficult to have back-gate controllability and may need even stronger field to have a reasonable amount of modulation. Since such large biasing can cause a significant increase of tunneling leakage at the drain region, special designs of drain may be needed [62].



(a)



(b)

Fig. 4.17. Substrate-bias controllability of the MOSFET and TFETs: (a) planar MOSFET with L =1 μm and W =10 μm, and (b) TFETs - NW-1 and NW-2 are nanowire TFETs in other chips. Planar in Fig.4.13(b) means the planar TFET. The dimensions of the planar TFET are same as those of the planar MOSFET. L and W of the nanowire TFET are 1 μm and 32.9 nm × 11 respectively. Here V_{DS} = –0.1 V.

Chapter 5

Conclusions

5.1 Conclusions

In this work, in order to provide a new ultralow power option for the future CMOS technologies, the conventional MOSFETs and nanowire TFETs were co-integrated and characterized.

For the fabrication of TFETs with improved performance, the nanowire active region scaled below 30 nm, ultrathin gate oxide with EOT < 3 nm, and dopant-segregated steep dopant profile were implemented. Using a novel self-aligned integration scheme for the asymmetric S/D, short-channel devices (min. L= 28 nm) could be fabricated. For the fabrication of the devices, additional module processes such as the reduced-repulsion EBL process for sub-20 nm resolution, chemical corner-rounding method, thin double-layer sidewall spacer process and two-step nickel SALICIDE process were developed.

Through the electrical test of fabricated devices, the successful co-integration of

MOSFETs and nanowire TFETs were confirmed. From the fabricated short-channel

Table 5.1. Summary of Results.

Items	Long Ch. TFET	Short Ch. TFET
gate length [nm]	1000	109
active width [nm]	32.9	19.5
minimum point swing [mV/decade]	46.64	93.7 (62.4)
minimum one-decade swing [mV/decade]	60.8	126
I_{ON} (V_{DS} = -0.5 V, V_{GS}-V_{OFF} = -0.5 V) [A/μm]	8.7×10^{-9}	*-
I_{OFF} (V_{DS} = -0.5 V, V_{GS} = V_{OFF}) [A/μm]	8.0×10^{-14}	*-
I_{ON}/I_{OFF}	5.8×10^{4}	*-
self-aligned integration?	No	yes
co-integration with conventional MOSFETs?	yes	yes

* The device failed while measuring the items.

TFETs, the short-channel effect of TFETs were experimentally investigated. This means that the short-channel effect will still remain as an important issue for the technology scaling even after TFETs are adopted. Key data from the best long-channel TFET and short-channel TFET are summarized in Table 5.1.

Due to the higher sensitivity of tunneling current to electric field, the back-gate controllability of TFET characteristics were found to be smaller than that of MOSFET's. Characteristics of nanowire TFET showed no controllability in the bias range studied in this work.

Finally, the study on the TFETs with different channel directions showed a directional dependence of the TFET characteristics. This result shows a new possibility to control the performance of TFETs using anisotropy of tunneling process.

5.2 Suggestions for Future Work

As the last part of this work, the remaining problems and the problems found in this work are to be discussed here.

First, one of the biggest challenges for TFETs is the weak current drivability. Although the device is aimed at low-power operation, the drivability of the device is 1000 times smaller than the specifications of the present Low STandby Power (LSTP) devices [63]. Uses of the narrow bandgap materials, the adjacent tunneling control region, and the anisotropy of tunneling process can be considered for this purpose. Considering the recent evolution of CMOS technology, III-V material or Ge can be also options to improve the drive current. From this respect, a systematic evaluation of required bandgap and the gains from each option may be worth exploring. On top of that, high gate capacitance to induce large band-bending is a prerequisite to obtain a large drive current as demonstrated in Chapter 2. Due to the gate leakage issue, the gate dielectric with EOT = 2.84 nm was used in this work. With high-κ insulators such as HfO_2 (κ = 20), ZrO_2 (κ = 20), and La_2O_3 (κ = 25), TFETs will be able to obtain better performances.

Secondly, the fabrication of scaled TFETs should be pursued more. Although the scaling of the device dimensions should continue, the scaling of EOT below 1 nm is not easy even with high-κ insulator [64]. Therefore, the device with a recessed channel may have to be considered although there are not many people looking at this for now. Since the dominant resistance component of a TFET is the tunneling resistance, the increase of

channel length will not aggravate the current drivability [65].

Finally, as explained throughout this work, the use of TFETs should go with MOSFETs. Investigations on how much MOSFET/TFET hybrid circuits will be energy-efficient over MOSFET-only circuits and what problem occurs with the introduction of TFETs will need more work.

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Appendixes

A. Table of wet etchants.

B. Tables of dry etch recipes.

C. Etch curve of ICP-plasma poly-Si etcher (3 year data).

D. SC-1 polymer removal test.

Appendix A: Table of Wet Etchants

* All unit of etching is angstrom [Å].

** Information on HSQ is for uncured one.

*** Data in this page is only for reference.

Chemical	1864 APM	115 APM	115 HPM	100:1 dHF	10:1 dHF	50150 BHF	50:1 BHF	Hot Phos.	4:1 SPM	7:1 BHF
Bath	**5-B**	**5-B**	**5-A**	**5-C**	**NA**	**13-C**	**NA**	**3-C**	**2-B 13-A**	**2-A 3-A**
Comp.	NH_4OH: H_2O_2:DI =1:8:64	NH_4OH: H_2O_2:DI =1:1:5	HCL: H_2O_2:DI = 1:1:5	HF:DI = 75:7000	HF:DI = 600:6000	NH_4F: HF:DI = 50:1:50	NH_4F: HF = 50:1	Pure H_3PO_4	H_2SO_4: H_2O_2 = 4:1	NH_4F:HF = 7:1
Temp. [℃]	**65**	**80**	**80**	25	25	25	25	**120**	**120**	25
Time [min]	10	10	10	1	1	1	1	1	10	1
Therm. ox	9.4	42.4		34	390	200	152.3			850
MTO	37	173		87					1.71	
TEOS	48	248		227		725				
HSQ**	120	550		>2500						
LP SiN	4	33						36		
LP poly-Si	19	79								
a-Si		90								
nnfc HDP	109			100		440				
etri LP ox				160						

Appendix B: Table of Dry Etch Recipes

* All unit of etching is angstrom [Å].

** No consideration of micro trenching or loading effect.

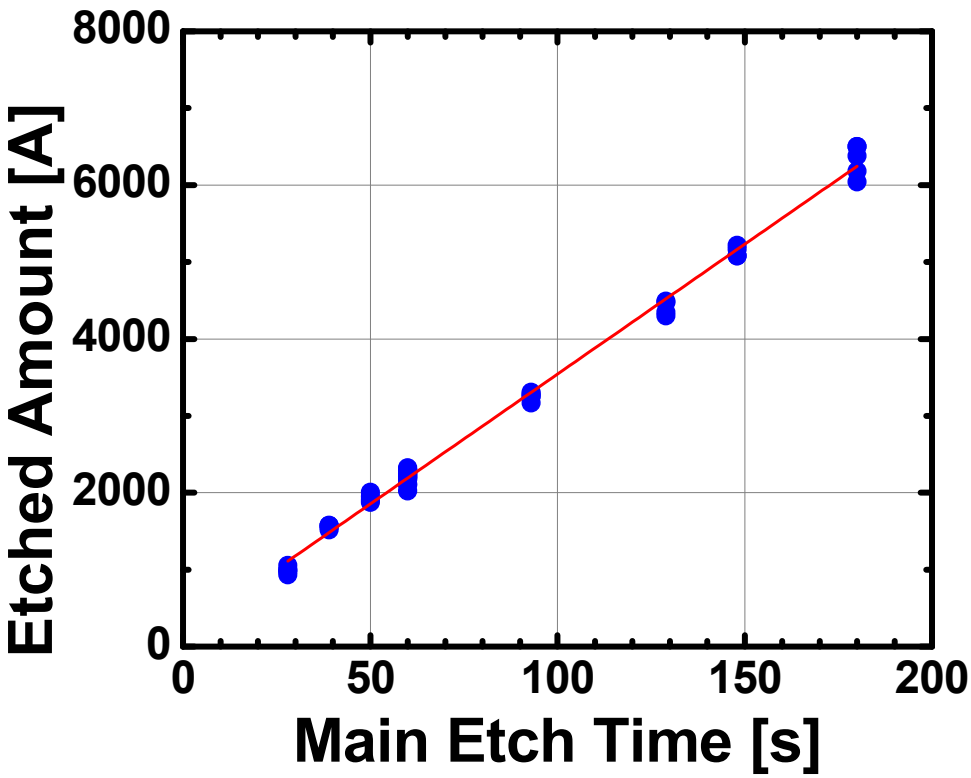
*** Data in this page is only for reference.

Recipes	Condition	Target Material	Equations (y =…)	Remark
STS 900/80 HBR	Standard: 3mT	Poly	33.952 t + 139.567	1200 Å/ 31 s
R: STI6IN	900W/80W w. CL2 10 s	SiN	2.921 t + 45.451	
STS 900/150 HBR	900W/150W w. CL2 10 s	Poly	40.034 t - 30.29	
STS 900/120 HBR	900W/120W w. CL2 10 s	Poly	31.73 t + 249.948	
STS 900/60 HBR	900W/60W w. CL2 10 s	Poly	28.308 t + 152.234	
STS 900/40 HBR	900W/40W w. CL2 10 s	Poly	33.567 t - 105.25	
STS 600/100 CL2	600W/100W	TEOS	8.301 t – 26.118	50 Å/ 10 s
		SiN	20.489 t + 15.229	
		Poly	20.489 t +15.229	
P5000IV	Standard:	TEOS	53.471 t – 57.264	1000 Å/ 20 s
R: SIO2_ETCH	130mT/600W/60G	HSQ	67.167 t – 121.769	
	CHF3/CF4/AR	POLY	5.247 t + 20.111	
P5000IV		NIT	72.357 t – 102.47	970 Å/ 15 s
R: NITRIDE				

Appendix C: Etch Curve of ICP-plasma Poly-Si Etcher (3-year Data).

* No consideration of micro trenching or loading effect.

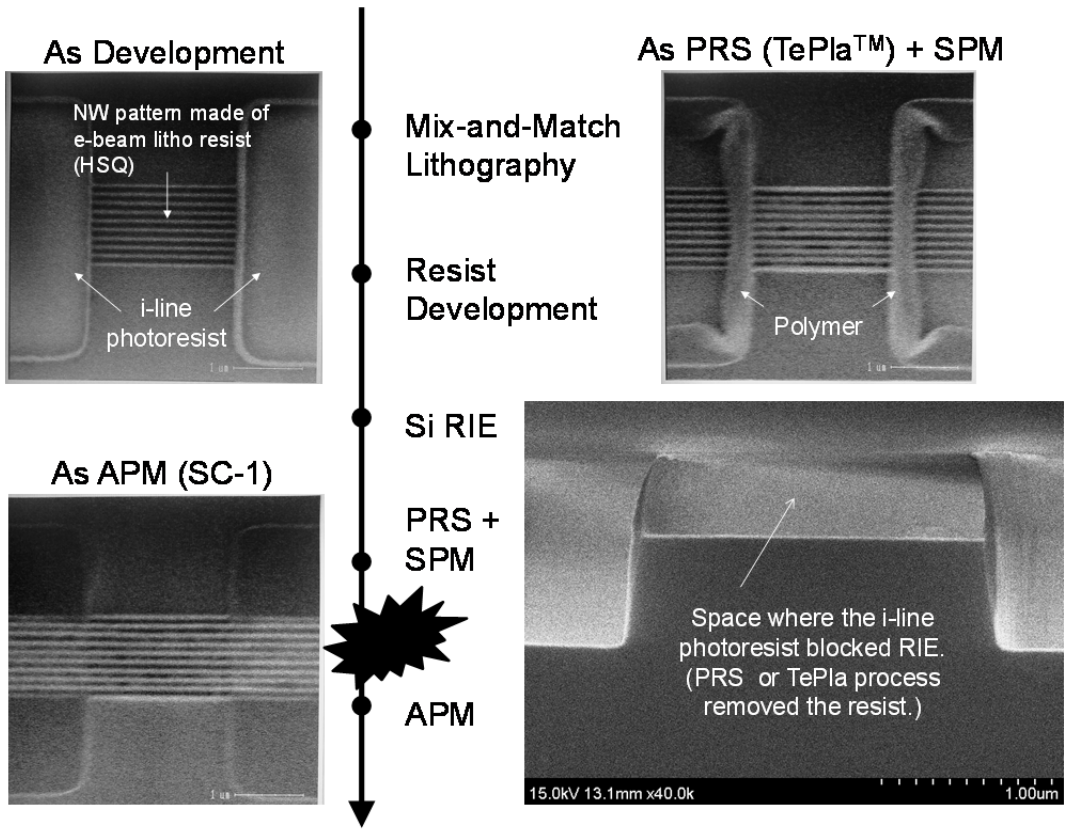
* Data in this page is only for reference.



$y = 33.952\ t + 139.567.$

Appendix D: SC-1 Polymer Removal Test

Polymer-like defects were observed along i-line resist edge after Si RIE/PRS/SPM. This defect is most likely from i-line photoresist and contains lots of carbon. SPM could not remove the defects. Either 115 APM @ 80℃ 3 min or 1864 APM @ 65℃ 6 min was enough to clean up these defects.



초 록

향후 CMOS 기술의 축소화에 따른 소자의 소비전력증가 문제를 해결하고 0.5 V 이하의 동작전압으로도 저전력 동작하는 스위칭 소자를 개발하기 위해, 기존 CMOS 기술을 변형한 집적방법으로 실리콘 나노와이어 밴드간-터널링 전계효과 트랜지스터(band-to-band tunneling field-effect transistor; TFET)와 금속-산화막-반도체 전계효과 트랜지스터(metal-oxide-semiconductor field-effect transistor; MOSFET)를 동시집적하고 소자로써 동작을 확인하였다.

TFET은 동작원리상 소스 영역의 에너지의 상한 값이 제한되어 있는 가전자대의 전자가 터널링에 의해 캐리어가 채널로 주입되므로 상온에서 MOSFET 보다 훨씬 작은 게이트 전압변화로 소자를 켤 수 있는 특징이 있다. 이 소자에서 터널링을 촉진하려면 소스/채널간 접합을 적은 공핍에도 쉽게 켤 수 있어야 하므로 게이트 산화막의 두께, 나노와이어의 선폭, 측벽 스페이서의 폭이 작아야 하고 접합주변에서 불순물 농도가 급격히 변해야 함을 이론적인 TCAD 시뮬레이션 연구를 통해 알 수 있었다.

이론적 연구를 바탕으로, 소스와 드레인의 극성이 서로 다른 TFET을 집적하기 위해 기존의 CMOS 집적방법에 자가정렬 비대칭 소스/드레인을 형성하는 집적방법 (integration scheme for self-aligned asymmetric source/drain)을 추가하여 MOSFET과 TFET을 SOI 기판 위에 동시집적

하였다. 최적화된 전자선 리소그래피공정 (electron-beam lithography)과 새로 개발한 화학적 코너 라운딩 (chemical corner-rounding) 방법을 적용하여 최소 선폭 14.5 nm의 반실린더형 나노와이어를 성공적으로 형성하였다. 측벽 스페이서는 질화막과 산화막으로 폭 20 nm로 형성하여, 액티브 영역의 손상을 최소화하여 자가정렬된 니켈 실리사이드 (self-aligned nickel silicide)를 형성하는데 문제가 없도록 하면서도 측벽 스페이서의 선폭을 최소화할 수 있도록 하였다. 접합의 농도가 급변하게 하기 위해서 니켈 실리사이드에 의한 스노플라우 효과 (snowploughing effect)를 이용하였다. 이를 통해 게이트 길이 1 μm인 장채널 TFET과 150 ~ 28 nm의 단채널 TFET들이 자기정렬 방식으로 성공적으로 제작되었다.

제작된 소자의 측정결과 n^+/진성 경계가 p^+/진성 경계에서보다 불순물 농도가 더 급격하도록 만들어진 것을 확인하였고, 따라서 TFET은 p-채널 모드로 더 잘 동작하였다. 장채널소자에서는 순간기울기 기준 47 mV/decade로 동작하는 소자가 만들어진 것을 확인하였으며, 단채널 TFET으로는 MOSFET의 경우처럼 채널길이가 짧아질 수록 게이트의 채널제어능력이 나빠지는 단채널효과가 TFET에도 존재함을 확인하였다. 단채널효과는 나노와이어의 선폭이 작아진 경우 감소하였는데 나노와이어 선폭 19.5 nm이고 게이트 선폭이 109 nm인 소자에서 62 mV/decade의 양호한 TFET 동작특성을 보였다. 이와 더불어 채널방향에 따른 소자 특성개선 가능성과 반실린더형 채널구조를 이용한 기판전압에 의한 소자특성 조절에 대한 가능성을 제작된 소자로부터 검토하였다.

이상의 결과에서 기존 CMOS 기술을 변형하는 방식으로 MOSFET과 TFET을 동시집적함으로써 좀 더 양산가능성 높은 TFET 제작 방법을 제시하였으며 향후 MOSFET-TFET 혼성회로를 이용한 미래 CMOS 회로의 저전력화 가능성을 제시하였다.

주요어: 밴드간-터널링 전계효과 트랜지스터, 나노와이어 트랜지스터, 자가정렬 비대칭 소스/드레인, 동시집적, CMOS 호환성, 0.5 V 이하 동작.

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“The light shines in the darkness, and the darkness has not overcome it.” - John 1:5.

Min-Chul Sun

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